International Journal of Multidisciplinary Engineering in Current Research
ISSN: 2456-4265, Volume 2, Issue 12, December 2017, http://ijmec.com/

Low Power, High Throughput, and Low Area Adaptive Fir Filter Based on Distributed Arithmetic

SALAGALA JAYA SREE, P.SANDHYA RANI
Mtech Scholar, Assistant Professor
Department of ECE
ISTS Women's Engineering College, Rajanagaram, Rajamahendravaram, A.P, India.

***Abstract*—This brief presents a novel pipelined architecture for low-power, high-throughput, and low-area implementation of adaptive filter based on distributed arithmetic (DA). The throughput rate of the proposed design is significantly increased by parallel lookup table (LUT) update and concurrent implementation of filtering and weight-update operations. The conventional adder-based shift accumulation for DA-based inner-product computation is replaced by conditional signed carry-save accumulation in order to reduce the sampling period and area complexity. Reduction of power consumption is achieved in the proposed design by using a fast bit clock for carry-save accumulation but a much slower clock for all other operations. It involves the same number of multiplexors, smaller LUT, and nearly half the number of adders compared to the existing DA-based design. From synthesis results, it is found that the proposed design consumes 13% less power and 29% less area-delay product (ADP) over our previous DA-based adaptive filter in average for filter lengths $N = 16$ and 32. Compared to the best of other existing designs, our proposed architecture provides 9.5 times less power and 4.6 times less ADP.**

***Index Terms*—Adaptive filter, circuit optimization, distributed arithmetic (DA), least mean square (LMS) algorithm.**

1 INTRODUCTION

Finite impulse response (FIR) digital filter is widely used as a basic tool in various signal processing and image processing applications The order of an FIR filter primarily determines the width of the transition-band, such that the higher the filter order, the sharper is the transition between a pass-band and adjacent stop-band. Many applications in digital communication (channel equalization, frequency channelization), speech processing (adaptive noise cancelation), seismic signal processing (noise elimination), and several other areas of signal processing require large order FIR filters. Since the number of multiply-accumulate (MAC) operations required per filter output increases linearly with the filter order, real-time implementation of these filters of large orders is a challenging task. Several attempts have, therefore, been made and continued to develop low-complexity dedicated VLSI systems for these filters

As the scaling in silicon devices has progressed over the last four decades, semiconductor memory has become cheaper, faster and more power-efficient. According to the projections of the international technology roadmap for semiconductors (ITRS), embedded memories will continue to have dominating presence in the system-on-chip (SoC), which may exceed 90%, of total SoC content. It has also been found that the transistor packing density of SRAM is not only high, but also increasing much faster than the transistor density of logic devices. According to the requirement of different application environments, memory technology has been advanced in a wide and diverse manner. Radiation hardened memories for space applications, wide temperature memories for automotive, high reliability memories for biomedical instrumentation, low power memories for consumer products, and high-speed memories for multimedia applications are under continued development process to take care of the special needs.

Interestingly also, the concept of memory, only as a standalone subsystem in a general purpose machine is no longer valid, since embedded memories are integrated as part within the processor chip to derive much higher bandwidth between a processing unit and a memory macro with much lower power-consumption. To achieve overall enhancement in performance of computing systems and to minimize the bandwidth requirement, access-delay and power dissipation, either the processor has been moved to memory or the memory has been moved to processor in order to place the computing-logic and memory elements at closest proximity to each other. In addition to that, memory elements have also been used either as a complete arithmetic circuit or a part of that in various application specific platforms.

2. MEMORY-BASED STRUCTURES

The phrase we use "*memory-based structures*" or "*memory-based systems*" for those systems where memory elements like RAM or ROM is used either as a part or whole of an arithmetic unit. Memory-based structures are more regular compared with the multiply-accumulate structures; and have many other advantages, e.g., greater potential for high-throughput and reduced-latency implementation, (since the memory-access-time is much shorter than the usual multiplication-time) and are expected to have less dynamic power consumption due to less switching activities for memory-read operations compared to the conventional multipliers. Memory-based structures are well-suited for many digital signal processing (DSP) algorithms, which involve multiplication with a fixed set of coefficients.

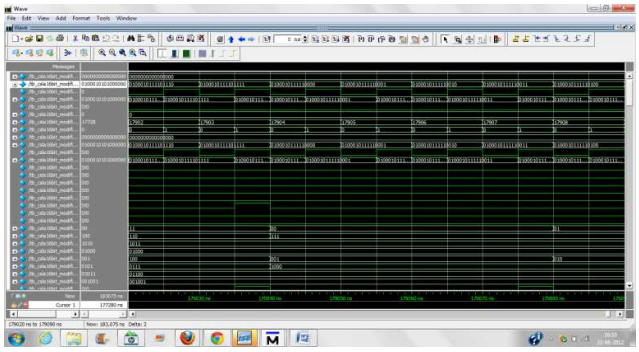
There are two basic variants of memory-based techniques. One of them is based on distributed arithmetic

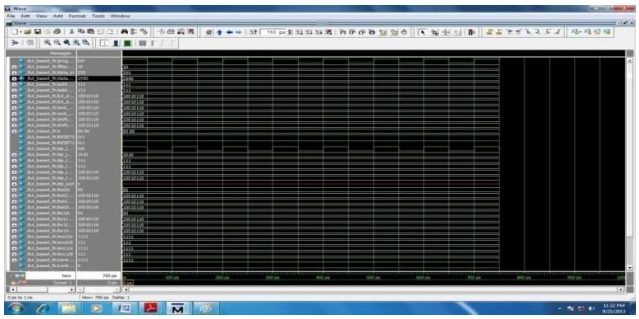
International Journal of Multidisciplinary Engineering in Current Research
ISSN: 2456-4265, Volume 2, Issue 12, December 2017, http://ijmec.com/

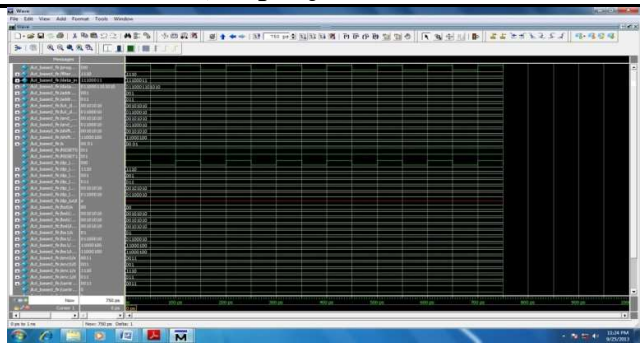
(DA) for inner product computation and the other is based on the computation of multiplication by look-up-table (LUT). In the LUT-multiplier-based approach, multiplications of input values with a fixed-coefficient are performed by an LUT consisting of all possible pre-computed product values corresponding to all possible values of input multiplicand, while in the DA-based approach, an LUT is used to store all possible values of inner-products of a fixed –N-point vector with any possible N-point bit-vector. If the inner-products are implemented in a straight-forward way, the memory-size of LUT-multiplier based implementation increases exponentially with the word length of input values, while that of the DAbased approach increases exponentially with the innerproduct- length. Attempts have been made to reduce the memory-space in DA-based architectures using offset binary coding (OBC) and group distributed technique. A decomposition scheme is suggested in a recent paper for reducing the memory-size of DA-based implementation of FIR filter. But, it is observed that the reduction of memorysize achieved by such decompositions is accompanied by increase in latency as well as the number of adders and latches.

3. SIMULATION RESULTS

The below figures shows the simulation results of test cases applied to the DUT. The response of the device for the control test case at the usb interface. The master transmitter sending random data to the external slave device.







4. CONCLUSION

We have suggested an efficient pipelined architecture for low-power, high-throughput, and low-area implementation of DA-based adaptive filter. Throughput rate is significantly enhanced by parallel LUT update and concurrent processing of filtering operation and weight-update operation. We have also proposed a carry-save accumulation scheme of signed partial inner products for the computation of filter output. From the synthesis results, we find that the proposed design consumes 13% less power and 29% less ADP over our previous DA-based FIR adaptive filter in average for filter lengths $N = 16$ and 32. Compared to the best of other existing designs, our proposed architecture provides 9.5 times less power and 4.6 times less ADP. Offset binary coding is popularly used to reduce the LUT size to half for area-efficient implementation of DA [2], [5], which can be applied to our design as well.

REFERENCES

[1]. Verilog HDL- Digital Design and Synthesis, by Samir Palnitkar
[2]. Open Cores project site http://www.opencores.org..
[3]. CISCO Integrated Services Router –SRND(Solution Reference Network Design) document
[4]. NORTEL ISP Router Design document.
[5]. VMM User guide
[6]. VMM Reference manual
[7]. System Verilog for verification by Chris Spear
[8]. Writing test benches using system Verilog by Janick Bergeron
[9]. OVM Cook book
[10]. OVM Reference manual
[11]. Websites
[12]. www.testbench.in
[13]. www.ovmworld.org
[14]. www.systemverilog.org
[15]. www.cisco.com/go/isr
[16]. www.vmmcentral.com