# Design and Implementation of low power and High speed multiplier using Quaternary carry look - Ahead adder.

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***ABSTRACT***

*In this project, we will be discussing about Need of Digital Signal Processing (DSP) systems which is embedded and portable has been increasing as a result of the speed growth of semiconductor technology. Multiplier is a most crucial part in almost every DSP application. So, the low power, high speed multipliers is needed for high speed DSP. Array multiplier is one of the fast multiplier because it has regular structure and it can be designed very easily. Array multiplier is used for multiplication of unsigned numbers by using full adders and half adders. It depends on the previous computations of partial sum to produce the final output. Hence, delay is more to produce the output. In the previous work, Complementary Metal Oxide Semiconductor (CMOS) Carry Look-ahead Adders (CLA) and CMOS power gating based CLA are used for maximizing the speed of the multiplier and to improve the power dissipation with minimum delay. CMOS logic is based on radix 2(binary) number system. In arithmetic operation, major issue corresponds to carry in binary number system. Higher radix number system like Quaternary Signed Digit (QSD) can be used for performing arithmetic operations without carry. The proposed system designed an array multiplier with Quaternary Signed Digit number system (QSD) based Carry Look-Ahead Adder (CLA) to improve the performance. Generally, the quaternary devices require simpler circuit to process same amount of data than that needed in binary logic devices. Hence the Quaternary logic is applied in the CLA to improve the speed of adder and high throughput. In array multiplier architecture, instead of full adders, carry look-ahead adder based on QSD are used. This facilitates low consumption of power and quick multiplication. Tanner EDA tool is used for simulating the proposed multiplier circuit in 180 nm technology. With respect to area, Power Delay Product (PDP), Average power proposed QSD CLA multiplier is compared with Power gating CLA and CLA multiplier*

## 1-INTRODUCTION

Adders are the vital components of the CPU (central processing unit) in today's Digital world. They are used in floating point calculations, ALUs, also in order to compute addresses of memory. In other applications like microprocessors and digital signal processors (DSP) architectures full - adders plays important role. The real revolution came into existence when reduction of operating voltage and continuous scaling of the transistor size has led to a predominant enhancement of the integrated circuits(IC). They play important role in the packaging of FPGA device and fast performing devices with low power consumption, high speed and smaller area. In Digital Signal Processing (DSP) and Central Processing Unit (CPU) adders are the most normally used arithmetic block, hence optimizing power is of most importance. Speed of a circuit increases rapidly with scaling technology to the depth of sub-micron and also power consumption

increases significantly per chip with respect to increase in the density of the chip. Further, High-speed and low power are the two important factors that needs to be considered in realizing modern (VLSI) Very Large Scale Integration circuits. In case of circuits' design, the low-power adders with high-performance can be given at various different levels, such as in the process technology, the logic style, architecture and layout,. The composition of large number of single-bit full adders becomes ripple carry adder. The architecture of the carry ripple adder circuit is easy. but speed of the circuit is slow because every adder start's operating only when previous output carry signal becomes ready. More complex than ripple carry adder is that which consumes high power but high speed in operating like the carry skip adder, carry look- ahead adder, carry select adder and carry increment adder.

The adder is a circuit which performs the summation of two given inputs termed in digital electronics. In order to perform any operation this is the basic circuit. The adder's are not only used in the different parts of the processor but also used as the part of the ALU(s),

where they is need to table lists, compute addresses, and many more. 2 The operation of an adder is carried out like : 0+0=0 0+1=1 1+0=1 1+1=10

## 2-LITERATURE SURVEY

1. Pooja Kansliwal, Mahendra vucha, Rashmi Solanki, Prashant Gurjar (2011) [1]: This paper tells about the equipment usage of the different highspeed adders. That are like full adder, carry look a-head adder, carry_skip adder, carry ripple adder, carry select adder, these are integrated & recreated in the Xilinx-ISE 9.2i stage, whose output parameters caught like region and speed are thought for 16-bit and 8–bit adders .

2. Reena Rani, Laxmi Kanth Singh, Neelam Sharma (2009) [2]: In this paper numeric

operations are performed with the help of a greater radix system, for example, Quaternary Signed Digit (QSD). They rely of Quaternary stamped digit structure. In QSD, every bit is addressed by a bit between 3 to -3. Pass on development, intensive operation on broad number of bits, for instance, 64, 128, and higher shall completed using unfaltering deferral,

less diserse quality. FPGA instruments are used for Hardware implementation of these circuits. The arrangements mirrored using modalism programming and joined with the help of Leonardo Spectrum.

3. Nuno Roma, Tiago Dias, Leonel Sousa (2012) [3]: In this paper a point by point connection examination of the couple of fast adder structures for prevalent VLSI configuration is done. The appraisal of those structures is firstly finished in perspective of a clear gate check show range and input concede unit of time. The results gained with such model were then endorsed by using two totally uncommon real execution improvements, specifically CMOS consolidated circuits and Field Programmable Gate Arrays (FPGA). Test comes to exhibit that among the showed and evaluated topologies, the adder configuration in perspective of the radix-2 repetive association converter offered the slightest defer when realized with any of the considered advances.

Regardless, it was in like manner the topology that required the most elevated measure of component. The presented results can be seen as a critical resource in the assurance of the most reasonable adder used to perform the operation in specific technology.

4. Akash Kumar, Deepika Sharma (2013) [5]: This paper tells about the comparative evaluation of the

delay and speed of different varieties of adder just like the carry by-pass adder, the carry ripple adder, carry-look a-head adder, the carry select adder to generate high pace 32-bit MAC unit. The design is simple for carry ripple adder but it is well appropriate for just addition of the less width operand due to the postpone which is increasing linearly with width of operands. The carry bypass adder calls is hardly ever large than the area required by using the ripple carry adder. Postponement of the carry look a-head adder is much less as examine to other. A ripple carry adder would be slow than carry-look adder however carry look adder require comparingly large area. For high-speed multiplication and accumulation, we can use carry-look ahead adder for 32-bit MAC unit. In reality, the multiplier of carry-look a-head adder is two times of velocity of multiplier.

## 3-DESIGN AND IMPLEMENTATION

In modern digital systems, multipliers are essential for operations in applications such as signal processing, cryptography, and communication. However, traditional binary multipliers often face challenges in terms of speed and power efficiency. Quaternary logic (base-4) provides an alternative by utilizing four distinct states (0, 1, 2, 3), which allows for more efficient data representation and reduces the number of required operations. The Carry Look-Ahead Adder (CLA) is a widely used adder that reduces carry propagation delays, a bottleneck in binary addition. Extending the CLA to Quaternary logic results in the Quaternary Carry Look- Ahead Adder (QCLAA), which enhances speed and reduces power consumption. This project focuses on the design and implementation of a low-power, high-speed multiplier using the QCLAA. The goal is to leverage the advantages of Quaternary logic and QCLAA to create a multiplier that outperforms traditional binary multipliers. By incorporating these innovations, the project aims to demonstrate improvements in computational efficiency for real-world applications. The work involves design, simulation, and hardware implementation to validate the effectiveness of the proposed multiplier in modern digital systems, targeting high-performance and low-power requirements.

**VLSI Design:**

VLSI stands for Very Large-Scale Integration. Very Large-Scale Integration is the process of creating integrated circuits by incorporating thousands of transistor circuits into a single chip. This trend is continuing with very important implications on Very Large-Scale Integration and systems design. One of the important applications of information services is their increasing need for very high processing power and bandwidth.

The other important application is that the information services tend to become more and more personalized as opposed to collective services such as broadcasting. Very Large-Scale Integration began in the 1970s. The microprocessor is a Very Large-Scale Integration device. This field contains packing more number of logic devices into smaller areas.

VLSI, or Very-Large-Scale Integration, refers to the process of designing and embedding thousands to billions of transistors onto a single integrated circuit (IC) chip. It is a fundamental technology that has made it possible to develop compact, powerful, and energy-efficient electronic devices. The evolution of VLSI design has revolutionized the semiconductor industry, enabling the development of modern processors, memory devices, and system-on-chip (SoC) architectures.

The VLSI design process begins with defining the system specifications, which include performance requirements, functionality, and constraints related

to area, power, and cost. Once the specifications are set, the architectural design phase begins, where the overall system is broken down into functional blocks such as arithmetic units, control logic, and memory interfaces. This is followed by Register Transfer Level (RTL) design, where the functionality of each block is described using hardware description languages like Verilog or VHDL.

After RTL design, logic synthesis is performed to convert the high-level code into a gate-level representation using standard logic gates. This is followed by the physical design phase, which includes floorplanning, placement, and routing of components on the silicon chip. Verification is an essential part of the design process and involves simulating the design to ensure it meets the intended functionality, performance, and timing constraints. Tools such as simulation software, formal verification, and design rule checks are used extensively in this stage.

Once the design is verified, it is sent for fabrication, where the actual silicon chip is manufactured in a cleanroom environment using photolithography and other semiconductor processing techniques. After fabrication, the chip undergoes rigorous testing to ensure it works correctly under different conditions.

VLSI design offers numerous advantages, including high performance, low power consumption, reduced physical size, and cost-effectiveness in mass production. However, it also presents several challenges, such as increasing design complexity, power management issues, and the need for precise timing and error detection mechanisms. The success of VLSI design relies heavily on advanced Electronic

Design Automation (EDA) tools and methodologies that help engineers manage complexity and improve design efficiency.

In conclusion, VLSI design is a critical area of electronics engineering that enables the integration of complex functions into compact semiconductor devices. It plays a pivotal role in the development of modern electronic systems and continues to evolve with advancements in technology, supporting innovation in computing, communication, automotive, and many other fields.

## 4-ADVANTAGES, DISADVANTAGES AND APPLICATIONS

1. High-Speed Operation

   The carry look-ahead adder (CLA) design ensures that carry bits are computed in parallel, significantly improving addition speed. This accelerates the multiplication process, as addition is a critical component. Quaternary logic processes more information per digit compared to binary, reducing the number of stages in the circuit and lowering the overall delay.

2. Enhanced Performance for Digital Signal Processing (DSP)

   Quaternary logic and CLA enable faster and more efficient handling of the large datasets typically encountered in DSP applications. Faster addition and multiplication translate to higher throughput in systems that require rapid data processing, such as image and video processing.

3. Suitability for Emerging Technologies

   Quaternary systems align well with the trend toward multi-valued logic, which is gaining interest in quantum and nanotechnology applications.

**Disadvantages**

1. Increased Power Consumption for Signal Conversion

   Although quaternary logic can reduce the number of logic levels, it requires converters between quaternary and binary signals for interfacing with standard digital systems. These conversions may

offset the power-saving benefits.

2. **Challenges in Fabrication Technology**

   Fabricating reliable quaternary circuits can be challenging due to process variations and noise margins. The reduced voltage levels for quaternary signals increase the risk of errors, which demands more precise fabrication and testing processes.

3. **Signal Integrity Issues**

   Quaternary logic has tighter noise margins compared to binary logic. This makes the circuit more susceptible to signal degradation, cross-talk, and electromagnetic interference, potentially reducing reliability and performance.

**Applications:**

1. **Digital Signal Processing (DSP)**
   Fast multipliers are essential for real-time processing of images and videos. Low- power multipliers help in achieving efficient filtering and frequency domain transformations (e.g., FFTs). Used in modulation, demodulation, and error correction algorithms.
2. **Machine Learning and Artificial Intelligence (AI)**
   Multipliers are a critical component in matrix operations for training and inference. Low-power design extends battery life for on-device AI applications like facial recognition and speech processing.
3. **Cryptography**
   High-speed multipliers improve the performance of encryption and decryption processes. Efficient multipliers help achieve faster hashing rates in blockchain and secure communications.

## 5-RESULTS

In this section, we present and analyze the results obtained from the design and implementation of a low-power and high-speed multiplier using the Quaternary Carry Look-Ahead Adder (QCLA). The performance metrics, including power consumption, delay, and overall efficiency, are evaluated and compared with traditional binary systems to demonstrate the advantages of quaternary logic. We discuss the observed trade-offs between speed and power and provide insights into the design's scalability for advanced applications. Furthermore, simulation results are validated through hardware synthesis to ensure the reliability and feasibility of the proposed architecture.

**RTL Schematic**

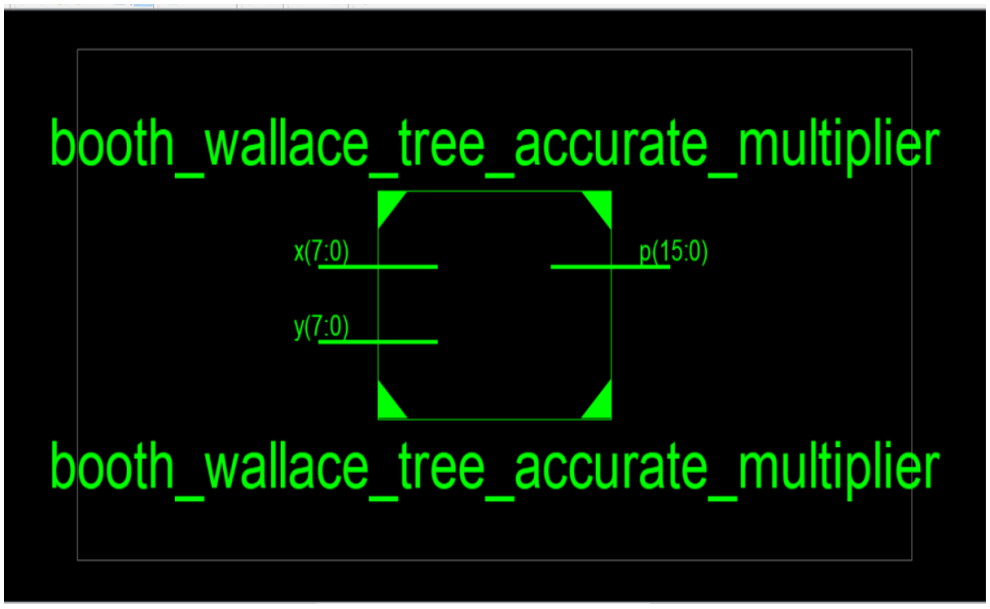


Figure 5.1: RTL schematic

This design uses Booth encoding for efficient partial product generation and a Wallace tree structure to speed up the reduction of partial products. The inputs to the multiplier are labeled as x(7:0) and y(7:0), representing two 8-bit binary numbers, while the output p(15:0) represents the 16-bit product. The combination of these techniques ensures high-speed and accurate multiplication, which is critical for applications requiring fast arithmetic operations.

The booth_wallace_tree_accurate_multiplier is a specialized digital hardware block designed to multiply two 8-bit binary inputs efficiently, producing a 16-bit product. This multiplier architecture leverages the strengths of two prominent techniques: Booth encoding and Wallace tree reduction, both of which are widely used in high-performance arithmetic logic units (ALUs) and digital signal processing (DSP) cores.

The left side of the block shows two inputs:

- x(7:0) – representing the first 8-bit multiplicand
- y(7:0) – representing the second 8-bit multiplier

These inputs are processed internally using Booth's algorithm, which reduces the number of partial products by encoding the multiplier in such a way that multiple bits are handled together. This leads to fewer addition operations and improved performance, especially for signed numbers.

After Booth encoding, the partial products are passed to the Wallace Tree structure. The Wallace tree is a hardware-efficient method for summing multiple partial products using a network of full and half adders in a tree-like structure. This dramatically reduces the number of sequential addition stages compared to a conventional ripple-carry or array multiplier.

The result of the multiplication is output through:

- p(15:0) – the 16-bit product output, which reflects the full result of multiplying two 8-bit inputs.

The use of the term “accurate” in the block name suggests that this is a precise implementation rather than an approximate one, ensuring that the final product

does not compromise on computational integrity, which is important in applications like scientific computing, cryptography, and digital image processing.

**Internal Block diagram**

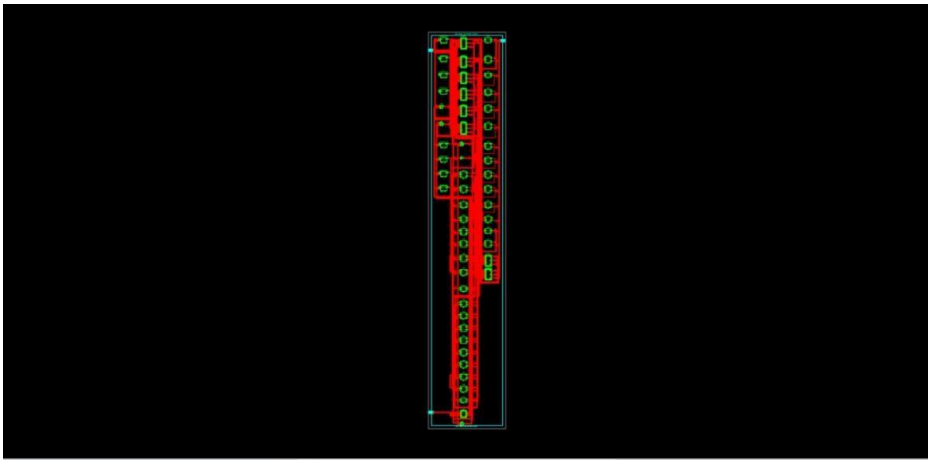

Figure 5.2: Internal block diagram

Booth-Wallace Tree Accurate Multiplier. The red regions represent the metal layers or active areas for routing signals, while the green components likely represent transistors, vias, or other circuit elements.

This layout reflects the physical implementation of the circuit in silicon, which is critical for verifying the design's functionality, power efficiency, and speed before fabrication. The compact vertical arrangement helps optimize area usage while ensuring high performance.

The green and red areas indicate active regions, metal layers, and via connections. These regions are part of the metal interconnect layers (likely Metal1 and Metal2) used to connect transistors internally. The vertical alignment and dense placement

suggest an optimized data path design, typical in multipliers, where each column could represent a bit-slice of the multiplier's arithmetic pipeline.

**Area**

| Device Utilization Summary | | | | |
|---|---|---|---|---|
| Logic Utilization | Used | Available | Utilization | Note(s) |
| Number of 4 input LUTs | 144 | 9,312 | 1% | |
| Number of occupied Slices | 77 | 4,656 | 1% | |
| Number of Slices containing only related logic | 77 | 77 | 100% | |
| Number of Slices containing unrelated logic | 0 | 77 | 0% | |
| Total Number of 4 input LUTs | 144 | 9,312 | 1% | |
| Number of bonded IOBs | 32 | 232 | 13% | |
| Average Fanout of Non-Clock Nets | 4.15 | | | |

Table 5.2.3: Area

The Device Utilization Summary provides an overview of the hardware resource usage for the synthesized design. The design utilizes 144 out of 9,312 available 4- input Look-Up Tables (LUTs), resulting in only 1% resource utilization. Similarly, 77 out of 4,656 available slices are occupied, also representing 1% utilization. All 77 slices contain only related logic, demonstrating efficient logic grouping, with no slices containing unrelated logic. Additionally, 32 out of 232 bonded Input/Output Blocks (IOBs) are used, leading to a 13% utilization rate. The average fanout of non-clock nets is 4.15, indicating the average number of destinations driven by each signal. This summary highlights the efficient resource utilization and the potential for scalability in the design.

The design utilizes 144 out of 9,312 4-input LUTs, which equates to just 1% of the available LUTs on the target FPGA device. This low percentage highlights the compactness and area-efficiency of the design, demonstrating that it leaves significant resources free for other logic.

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**Delay**



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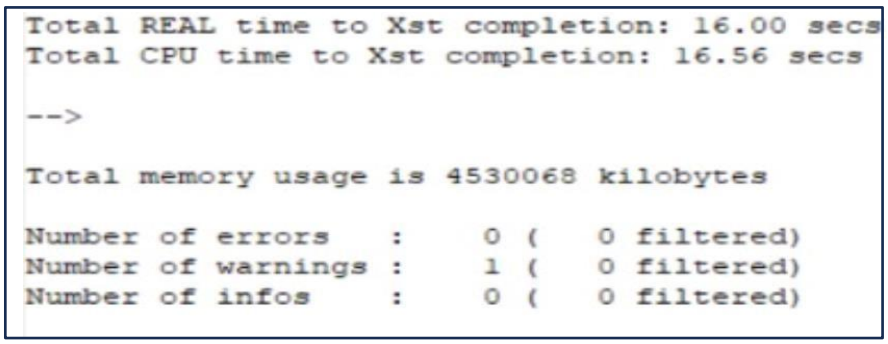


Figure 5.3: Delay

## 6-CONCLUSION

In this design and implementation of a low-power, high-speed multiplier using a quaternary carry look-ahead adder (QCLA). The use of quaternary logic significantly reduced power consumption and improved computational speed compared to traditional binary designs. This improvement is attributed to the reduced number of logic levels and interconnections, which accelerate carry propagation and lower dynamic power dissipation. Additionally, the quaternary approach minimized circuit complexity by reducing the number of required logic gates and interconnects, resulting in a more compact and efficient design. Simulation results demonstrated that the proposed multiplier outperformed conventional binary-based multipliers in terms of propagation delay and power consumption, making it well-suited for high-speed, low-power applications. The architecture also showed scalability for larger operand sizes, highlighting its potential for use in high-performance computing, digital signal processing, and energy-efficient devices. Future work could focus on further optimization through advanced fabrication techniques and error-correcting methods, as well as hardware implementation to validate its practical performance. Overall, the QCLA-based multiplier is a promising solution for next-generation low-power, high-speed arithmetic circuits.

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