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# Design and Validation of High Performance SRAM with High Recoverability of Multinode Soft Error

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***ABSTRACT***

*With the advancement of technology, the size of transistors and the distance between them are reducing rapidly. Therefore, the critical charge of sensitive nodes is reducing, making SRAM cells, used for aerospace applications, more vulnerable to soft-error. If a radiation particle strikes a sensitive node of the standard 6T SRAM cell, the stored data in the cell are flipped, causing a single-event upset (SEU). Therefore, in this paper, a Soft-Error-Aware ReadStability- Enhanced Low Power 12T (SARP12T) SRAM cell is proposed to mitigate SEUs. To analyze the relative performance of SARP12T, it is compared with other recently published soft-error- aware SRAM cells. All the sensitive nodes of SARP12T can regain their data even if the node values are flipped due to a radiation strike. To estimate the proposed LP10T SRAM cell's performance, it is compared with some state-of-the-art SRAM cells using HSPICE in 16-nm CMOS predictive technology model Furthermore, SARP12T can recover from the effect of single event multi-node upsets (SEMNUs) induced at its storage node pair. Along with these advantages, the proposed cell exhibits the highest read stability, as the '0'storing storage node, which is directly accessed by the bit line during read operation, can recover from any upset. Furthermore, SARP12T consumes the least hold power. SARP12T also exhibits higher write ability and shorter write delay than most of the comparison cells. All these improvements in the proposed cell are obtained by exhibiting only a slightly longer read delay and consuming slightly higher read and write energy.*

## 1-INTRODUCTION

The aerospace industry has made human lives simpler and improved security by providing a plethora of utilities, such as satellite communications, military surveillance, guidance, tracking systems, etc. In aerospace applications, microprocessors are widely used for control and guidance, engine control, inertial navigation, etc., and these processors are being embedded with multiple cores to upgrade their performance. A larger number of cores implies that a higher amount of cache memory is required.

Hence, SRAM cells, which are used as cache memory, play a vital role in the power, area, and delay optimization of the processor. Deep space contains highly energetic particles, which impact the functionality of memory circuits. On striking the substrate of an integrated circuit, such as semiconductor memory, an energetic particle generates electron-hole pairs. The electric field caused due to the reverse bias between the diffusion region and substrate/n-well appears to the strike generated minority carriers as a forward field. Hence, minority carriers drift towards the drain diffusion regions, and on accumulation, a positive or negative voltage spike is generated based on the type of minority carrier.

If the level of the spike is beyond the switching threshold of the logic circuit and its duration is long enough, the stored content may flip, resulting in a

phenomenon called single-event upset (SEU) or soft-error, Furthermore, with minimum spacing between devices of an integrated circuit decreasing drastically due to aggressive technology scaling, a strike by a single ion may affect multiple nodes, which may result in a single-event multinode upset (SEMNU). To address the effects of SEUs on memory, triple modular redundancy (TMR) has been used. This method uses three copies of memory cells, with majority voting to select and output the correct value. If one copy is flipped, the other two will dominate the voting process, resulting in the same output. However, this technique incurs huge area and power penalties, making it unsuitable for most designs. Another way to mitigate the effects of SEUs is to employ error correction codes (ECCs). However, ECCs incur huge power, area and delay overhead due to the requirement of redundancy and extra devices for encoding and decoding circuits. Therefore, soft-error-aware SRAMs are preferred over ECCs because they are a less power-area- and delay-consuming solution. Furthermore, it is preferred that the SRAM cell should have multi-node upset recoverability along with its SEU recovery ability.

The fully differential 10T SRAM cell presented in has increased the RSNM using the read decoupling technique. However, this cell shows poor WSNM due to the presence of two serially transistors in its write paths and consumes high read/write power, attributed to its dualended Bit-lines structure. A differential writing 10T (10T-P1) SRAM cell has been proposed in, which employs a data independent read port to reduce Bit-line leakage. This cell improves/increases RSNM/read delay and also suffers from low WSNM. However, RSNM of this cell is low due to lack of read decoupling technique. In this paper, we introduce a low standby power 10T (LP10T) SRAM cell with high static noise margins.

## 2-LITERATURE SURVEY

The miniaturization of CMOS technology has increased the vulnerability of memory cells to radiation-induced single-event upsets (SEUs), posing significant reliability challenges. To address this, a novel 12-transistor radiation-hardened memory (RHM) cell is proposed, offering 100% fault tolerance against SEUs and enhanced resilience to multiple-node upsets. The design is optimized for 65-nm CMOS technology and evaluated for access times, power consumption, and area efficiency, outperforming existing solutions. Monte Carlo simulations confirm its reliability under process, voltage, and temperature variations, making it ideal for critical applications in radiation-prone environments. This work advances fault-tolerant memory design for nano-scale technologies. The different configurations of SRAM cells have been designed to address existing challenges. In, a Schmitt-trigger-based 10T SRAM cell has been designed and proposed to improve both RSNM and WSNM simultaneously to overcome process variations.

Recent studies have explored 10T and 12T SRAM designs that include separate read and write paths to isolate sensitive nodes, thereby improving the Read Static Noise Margin and overall stability. These designs also reduce the probability of soft error propagation during memory access operations. Furthermore, use of redundancy and error-correcting codes has been studied as a system-level solution to complement hardening at the cell level.

The use of simulation and validation tools like Tanner Electronic Design Automation, SPICE, and Cadence is commonly adopted to evaluate critical metrics such as power, delay, noise margin, and error recovery under fault injection. Tools for Layout Versus Schematic (LVS) checking and Design Rule Checks ensure that the robust memory cells conform

to manufacturing constraints while preserving fault-tolerance.

These advancements collectively inform the present work, which focuses on designing a 12T SRAM cell optimized for high-performance and high recoverability from multinode soft errors.

The goal is to validate this design using physical layout tools, ensuring it meets the demands of low-power, high-speed applications in aerospace, defense, and mission-critical systems.

**Soft Error Hardened Memory Design for Nano-scale Complementary Metal Oxide Semiconductor Technology**

Radiation-induced single event upsets (SEUs), or soft errors, have become a dominant factor in the reliability degradation of Nano-scale memories. In this paper, based on the SEU physics mechanism, and reasonable layout-topology, a novel soft error hardened memory cell is proposed in 65 nm Complementary Metal Oxide Semiconductor (CMOS) technology. The design comparisons for several hardened memory cells in terms of access time (read access time and write access time), power consumption, and layout area are also executed. The main advantage of the proposed cell is that it can provide 100% fault tolerance, which is very useful for memory applications in severe radiation environments. Furthermore, Monte Carlo simulations are carried out to evaluate the effects of process, voltage, and temperature (PVT) variations. From simulations, we confirmed that the proposed cell has exhibited a sufficient multiple-node upset tolerance capability even under PVT variations SINGLE event upsets (SEUs) induced by radiation particles .

This literature survey highlights the growing significance of radiation-induced single event upsets (SEUs) in the degradation of reliability in nanoscale CMOS memory technologies. As technology nodes scale down, SEUs have emerged as a dominant reliability threat, especially in mission-critical and aerospace applications. To counter this, the surveyed work presents a novel Soft Error Hardened Memory (SEHM) cell design using 65 nm CMOS technology. This proposed design is evaluated based on several key performance parameters such as read access time, write access time, power consumption, and layout area. One of the primary strengths of the proposed memory cell is its capacity to offer 100% fault tolerance under severe radiation conditions. To ensure robustness, Monte Carlo simulations are employed to examine the memory cell's response to process, voltage, and temperature (PVT) variations. These simulations confirm the cell's high multi-node upset tolerance, meaning it can resist multiple bit flips caused by energetic particle strikes. Importantly, even under extreme PVT variations, the cell maintains immunity to single event upsets, making it highly suitable for IoT and aerospace environments where reliability is paramount.

**Design of Area-Efficient and Highly Reliable RHBD 10T Memory Cell for Aerospace Applications**

In this brief, based on upset physical mechanism together with reasonable transistor size, a robust 10T memory cell is first proposed to enhance the reliability level in aerospace radiation environment, while keeping the main advantages of small area, low power, and high stability. Using Taiwan Semiconductor Manufacturing Company 65-nm CMOS commercial standard process, simulations performed in Cadence Spectre demonstrate the ability of the proposed radiation-hardened-by-design 10T cell to tolerate both $0 \rightarrow 1$ and $1 \rightarrow 0$ single node upsets, with the increased read/write access time. SRAMs have been widely adopted in various aerospace electronic systems, and play a major role in the delay, area, power, and critical reliability. In

aerospace applications, SRAMs have a key constrain that makes a challenge in the reliability induced by energetic particles. Therefore, single event upsets (SEUs) are a major reliability failure mechanism that can cause a malfunctioning of an electronic system by

altering the stored value temporarily.

## 3-SOFTWARE REQUIREMENTS

Tanner EDA is a suite of tools for the design of integrated circuits. These tools allow you to enter schematics, perform SPICE simulations, do physical design (i.e., chip layout), and perform design rule checks (DRC) and layout versus schematic (LVS) checks. There are 3 tools that are used for this process: S-edit – a schematic capture tool T-SPICE – the SPICE simulation engine integrated with S-edit L-edit – the physical design tool Using S-Edit (Schematic Entry Tool) & T-SPICE (Analog Simulation Tool).

**Start New Design & Setup Libraries**

Initially Setup your Directory Structure & download Libraries a) Log onto a computer on 6th floor Cob Leigh. You want to create a directory for all of your Tanner EDA projects. You also will need to download and unzip a set of library & model files from the course website that will be used for your simulations.

Create a directory structure named "EELE414_VLSI_Fall2011\Tanner Projects c) Go to the course website and download the zip file called "Tanner_Libraries.zip". Unzip it into your Tanner Projects directory. These groups of files contain the necessary information to enter components into S-edit (circuit symbols), perform SPICE simulations (models), and do physical layout (layer definitions, DRC, LVS).

a) Start S-Edit: -
   Start – All Programs – Tanner EDA – Tanner Tools v12.6 – S-Edit v12.6
b) Start a New Design
c) Create a new Cell
d) Enter the Symbol Libraries

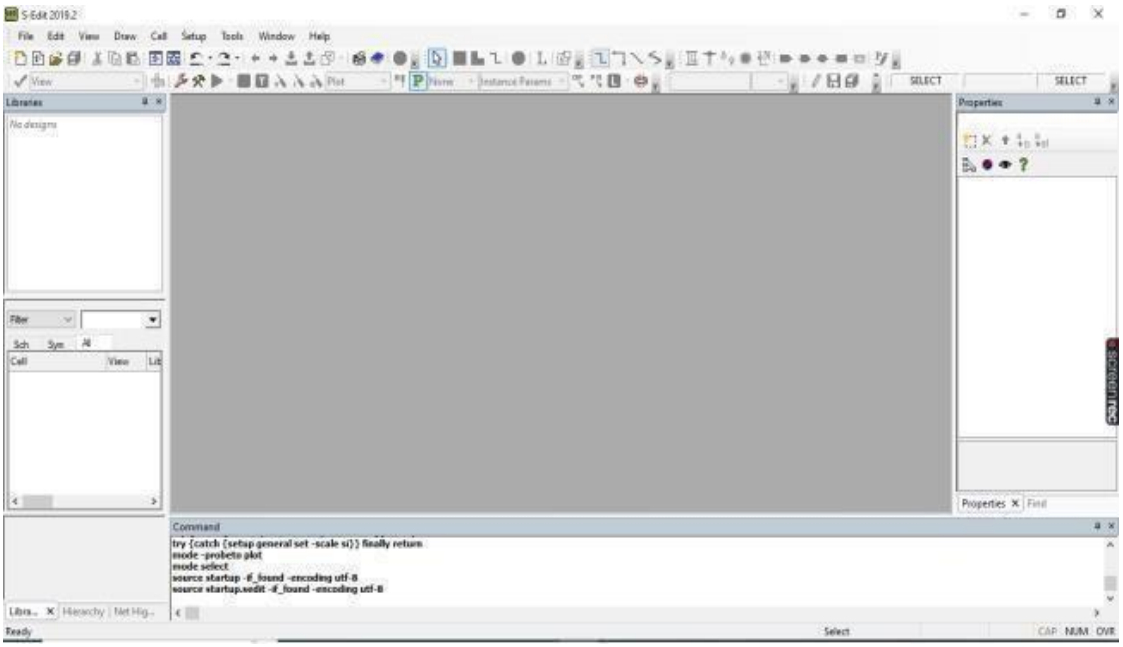


**Figure 3.1:** Start of new design and setup libraries

**Setup The SPICE Models for The GENERIC_025 KIT**

You will need to setup the SPICE models for this process in S-edit. Once you do that, when you enter an NMOS or PMOS transistor, you can then associate the 0.25um model to that symbol. Using the pull-down menus, setup the SPICE models: - Setup – SPICE Simulation – In the dialog that appears, you should highlight "General" on the left. – On the right, click in the "Library Files" field. This is where you will specify any SPICE models you will be using in your simulations.

Browse & select "Generic_025_Kit\ Generic_025_SPICE_Models_Level1.lib" – On the right, click in the "SPICE File Name" field. This is where you specify the name and location of the SPICE Net list output. Browse to your design directory "EELE414_VLSI_Fall2011\Tanner Projects\HW03_NMOS_IV_Part1" and enter the filename "Top's". – On the right, click in the "Simulations Results File Name" field. This is where the results of the simulation will be written. This file is what the waveform viewer will look for when you go to plot your results.

Browseto your design directory "EELE414_VLSI_Fall2011\Tanner Projects\HW03_NMOS_IV_Part1" and enter the filename "TOP. Out". Before you can exit this window, you will need to select an analysis type. We will setup the details of the analysis later, but for now, just check the "DC Sweep Analysis" and click "OK" to close the setup window.

**Enter The Schematic To Simulate The IV Behaviour Of An NMOS Transistor**

We will be entering the following circuit:

Enter the NMOS transistor – On the left, click on "Devices" in the upper window. This will display all of the symbols available in this group. You should see all of the components that you can implement on a CMOS integrated circuit. – On the bottom left window, click once on "NMOS". You should see the symbol of the NMOS transistor show up in the symbol viewer window at the bottom. – To place the NMOS, you will insert- "Instance" button. Two things happen when you click on this button. First, a dialog will appear that will allow you to setup the parameters for the NMOS. Second, the symbol will attach to your mouse.

## 4-METHODOLOGY WISE ANALYSIS

**Soft Error Hardened Memory Design for Nano-scale Complementary Metal Oxide Semiconductor Technology**

Radiation-induced single event upsets (SEUs), or soft errors, have become a dominant factor in the reliability degradation of Nano-scale memories. In this paper, based on the SEU physics mechanism, and reasonable layout-topology, a novel soft error hardened memory cell is proposed in 65 nm Complementary Metal Oxide Semiconductor (CMOS) technology. The design comparisons for several hardened memory cells in terms of access time (read access time and write access time), power consumption, and layout area are also executed.

The main advantage of the proposed cell is that it can provide 100% fault tolerance, which is very useful for memory applications in severe radiation environments. Furthermore, Monte Carlo simulations are carried out to evaluate the effects of process, voltage, and temperature (PVT) variations. From simulations, we confirmed that the proposed cell has exhibited a sufficient multiple-node upset tolerance capability even under PVT variations SINGLE event upsets (SEUs) induced by radiation particles resulting from packaging materials and Unfortunately, the writing speed, as well as write margin, of them is deteriorated. For low power and

highly reliable radiation-hardened application, the RH memory (RHM)-12T was proposed; however, the authors used nMOS as pull-up devices causing worse read noise margins.

**Soft errors rate mitigation techniques for modern Microcircus**

A unique circuit hardening technique is described, which can totally eliminate both alpha ,and'neutmn induced soft errors from deep submicron microcircuits. This hardening technique, termed temporal sampling, addresses both traditional static latch SEUs (single event upsets) as well as SET (single event transient) induced errors.

This approach mitigates the SER (soft error rate) of modem microcircuits with minimal impact on design flow, physical layout area, and circuit The alpha particle and cosmic ray induced SER in microcircuits has become increasingly imp6rtant in commercial microcircuits, as device feature sizes have decreased Alpha particles typically originate from the radioactive decay of impurities within the High energy neutrons are also known to produce upsets and transients in deep submicron microcircuits indirectly through elastic scattering and nuclear reactions within the silicon .

In these cases, a heavy ion recoil reaction hyproduct passes through a junction and produces a similar charge collection current pulse. On earth or on high altitude aircraft, high energy neutrons are encountered as reaction byproducts found in cosmic ray showers formed when an energetic heavy ion from space undergoes a nuclear reaction in the Temporal sampling has been successfully used in recent space become microelectronics applications and is easily adapted to terrestrial and high altitude environments .

In this paper, we will take the basic temporal sampling methodology and evolve it into practical circuit embodiments that are easily realizable in terrestrial, high altitude, and spacebome microcircuit designs. In particular, we will show how temporal sampling, in its most elegant application, can achieve the equivalent of triplesoatial redundancy without the ~~ II atmosphere. Necessity of physically replicating the actual circuitry. Finally, the size and speed tradeoffs of tempord sampling are discussed. On earth or on high altitude aircraft, high energy neutrons are encountered as reaction byproducts This hardening technique, termed temporal sampling, addresses both traditional static latch SEUs (single event upsets) as well as SET (single event transient) induced errors.

**Improving Error Correction Codes for Multiple-Cell Upsets in Space Applications**

Currently, faults suffered by SRAM memory systems have increased due to the aggressive CMOS integration density. Thus, the probability of occurrence of single-cell upsets (SCUs) or multiple-cell upsets (MCUs) augments. One of the main causes of MCUs in space applications is cosmic radiation. A common solution is the use of error correction codes (ECCs). Nevertheless, when using ECCs in space applications, they must achieve a good balance between error coverage and redundancy, and their encoding/decoding circuits must be efficient in terms of area, power, and delay. Different codes have been proposed to tolerate MCUs. For instance, Matrix codes use Hamming codes and parity checks in a bidimensional layout to correct and detect some patterns of MCUs.

Nevertheless, this size decreasing has also caused an augment in the memory fault rate. With the present aggressive scaling, the memory cell critical charge and the energy needed to provoke a single-event upset (SEU) in storage have been reduced. As shown by different experiments, in addition to traditional single-cell upsets (SCUs), this energy reduction can

provoke multiple-cell upsets (MCUs), that is, simultaneous errors in more than one memory cell induced by a single particle hit. In the case of space applications

**5-DESIGN IMPLEMENTATION & RESULT OF 12T SRAM**

The schematic of SARP12T and its equivalent layout .SARP12T has two word lines, WL and WWL, two storage nodes, Q and QB, and two internal nodes, S1 and S0. WL controls the access transistors N7 and N8, which connect the storage nodes Q and QB with their corresponding bit lines BL and BLB. The internal nodes S1 and S0 are connected to their corresponding bit lines BL and BLB through their corresponding access transistors N9 and N10, which are controlled by WWL.

Let us contemplate SARP12T and all the comparison cells storing '1', i.e., Q = '1' and QB = '0'. Thus, S1 and S0 are storing '1' and '0', respectively. With this consideration, the basic operations and SEU recovery analysis of SARP12T are explained below. A. Basic Operations All the basic operations of the proposed SARP12T are mentioned in this subsection. Hold Operation: During hold mode, both pairs of access transistors are kept OFF by pulling down both WL and WWL to GND..

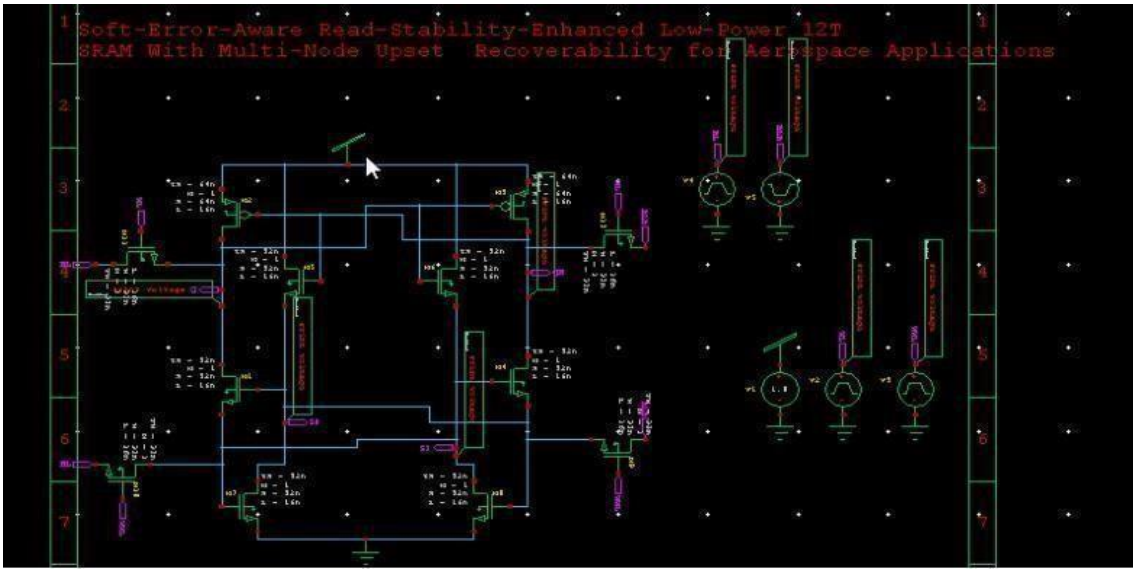



**Fig 5.1** 12 SRAM with multi-node soft error

Therefore, while the cell is in the hold state, transistors P1, N2, N3 and N6 remain ON, while the rest of the transistors remain OFF for the considered case. Thus, SARP12T maintains its initial stored data (Fig. 3). 2) Write Operation: During write operation, both the wordlines (WL and WWL) are activated. Therefore, both pairs of access transistors (N7/N8 and N9/N10) are turned ON.

For altering the stored data (i.e., writing '0' at Q), BL is connected to GND, whereas BLB is clamped at VDD. As BL is connected to GND, nodes Q and S1 are pulled down by BL through N7 and N9, respectively. Subsequently, node Q turns ON P2 and turns OFF N6, whereas node S1 turns OFF N2 and N3.

In the meantime, nodes QB and S0 are pulled up by BLB through N8 and N10, respectively. Consequently, node QB turns OFF P1 and turns ON N5. Similarly, node S0 turns ON N1 and N4. The cross-coupling between P1 and P2 amplifies the potential difference between Q and QB. Similarly, the cross-coupling between N3 and N4 enhances the

potential difference between S1 and S0. Therefore, the write operation is performed successfully .

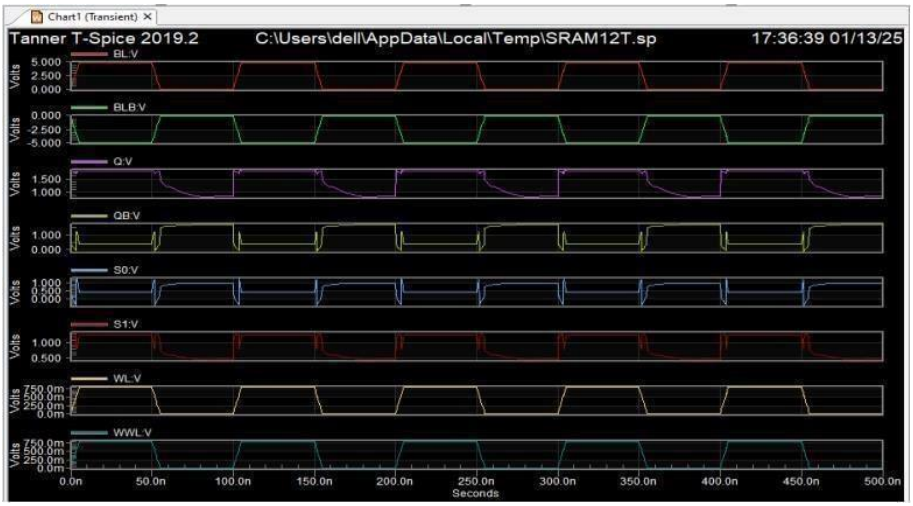



**Fig 5.1.1** 12 simulation results of SRAM with multi-node soft error

During read operation, WL is connected to VDD, whereas WWL is kept deactivated. Therefore, access transistors N7 and N8 are turned ON, while the other access transistors (N9 and N10) remain OFF.

Write "0" operation

WL=1,WWL=1,BL=0,BLB=1,Q=0,S1=0,QB=1,S0=1

Read Operation

WL=1,WWL=0,BL=1(PRECHARGED),BLB=0,Q=1,S1=1,QB=0,S0=0

For read operation, bit-lines are pre-charged to VDD. Therefore, BLB discharges through N8, N2 and N3. On the other hand, as N1 and N4 are OFF, BL stays at VDD (Fig. 3). Once the voltage difference between BL and BLB reaches 50 mV, a sense amplifier (not shown)

can sense the stored data, which completes the read operation.

**Basic Operations**

All the basic operations of the proposed SARP12T are mentioned in this sub-section.

**Hold Operation:**

During hold mode, both pairs of access transistors are kept OFF by pulling down both WL and WWL to GND. In order to shorten the read delay, bit lines are kept pre charged to VDD during hold mode. Therefore, while the cell is in the hold state, transistors P1, N2, N3 and N6 remain ON, while the rest of the transistors remain OFF for the considered case. Thus, SARP12T maintains its initial stored data.

**Write Operation:**

During write operation, both the wordlines (WL and WWL) are activated. Therefore, both pairs of access transistors (N7/N8 and N9/N10) are turned ON. For altering the stored data (i.e., writing '0' at Q), BL is connected to GND, whereas BLB is clamped at VDD.

As BL is connected to GND, nodes Q and S1 are pulled down by BL through N7 and N9, respectively. Subsequently, node Q turns ON P2 and turns OFF N6, whereas node S1 turns OFF N2 and N3.

In the meantime, nodes QB and S0 are pulled up by BLB through N8 and N10, respectively. Consequently, node QB turns OFF P1 and turns ON N5. Similarly, node S0 turns ON N1

and N4. The cross-coupling between P1 and P2 amplifies the potential difference between Q and QB. Similarly, the cross-coupling between N3 and N4 enhances the potential difference between S1 and S0. Therefore, the write operation is performed successfully .

**Simulation Result**

**Table 5.5** Simulation Result of 12T SRAM

| S.NO | METHOD | METHODOLOGY | NO OF TRANSISTOR | AVG POWER | DYNAMIC-POWER | STATIC POWER |
|---|---|---|---|---|---|---|
| 1 | SRAM-12T | EXISITNG METHOD | 12 | 4.463027e+00 | 1.975302e-02 | 9.158638e+00 |

The table presents performance data for a memory design technique labeled as "SRAM12T," which follows an existing methodology. The "12T" indicates that the design uses 12 transistors. The average power consumption of this design is reported as approximately

4.463 W (watts). Additionally, the power consumption is broken down into dynamic power and static power components. The dynamic power, which accounts for the power used during switching activity, is about 0.01975 W, while the static power, representing the power consumed when the circuit is idle, is significantly higher at approximately 9.159 W. This data suggests that static power dominates the overall power consumption in this method.

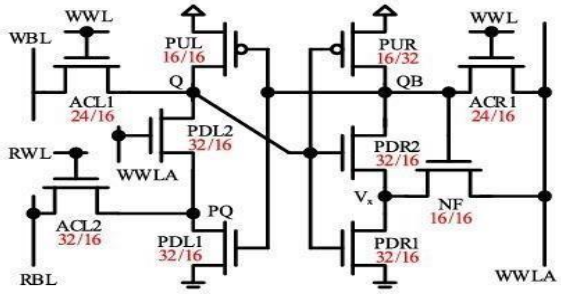
## 6-DESIGN IMPLEMENTATION & RESULT OF 10T SRAM

**Proposed method**

The two lines between the inverters are connected to two separate bit-lines via two nchannel pass-transistors (left and right of the cell). The gates of those transistors are driven by a word-line. In a larger SRAM, the word-line is used to address and enable all bits of one memory word (e.g., all 32 bits at address 0xcafe from a 64Kx32 SRAM chip). As long as the word-line is kept low, the SRAM cell is disconnected from the bit-lines. The inverters keep feeding themselves, and the SRAM stores its current value.

When the word-line is high, both n-channel transistors are conducting and connect the inverter inputs and outputs to the two vertical bit-lines. That is, the two inverters drive the current data value stored inside the memory cell onto the bit-line (left) and the inverted data value on the inverted bitline (right).

This data can then be amplified and generates the output value of the SRAM cell during a read operation.



The schematic of the proposed LP10T SRAM cell is shown in Figure 6.1. The core of the proposed LP10T SRAM cell consists of a cross-coupled structure of a standard inverter with a stacked transistor (PUL, PDL1, and PDL2) and a Schmitt trigger-based inverter (PUR, PDR1, PDR2, and NF). The cell core maintains the content of the true internal storage nodes Q and QB. The ACL1 and ACR1 are the write access transistors, which are controlled by row- based write word line (WWL). The ACL2 is the read access transistor, which is gated by rowbased read word line (RWL).

The column-based control signal (WWLA) controls the read/write assist transistor PDL2, which is placed between Q and pseudo Q (PQ) nodes. Furthermore, it is connected to the drain of the NF transistor. The proposed cell uses separate bitlines including column-based RBL and WBL for read and write operation, respectively. Table I shows the status of the various control signals employed in the proposed LP10T SRAM cell design for different operations.

The ST 10T and proposed ST 9T SRAM cells improve the read stability through the benefit of ST inverter. Furthermore, the proposed ST 9T SRAM cell has a larger read stability than ST 10T SRAM cell where the ST inverters are cross-coupled. The reason is as follows. When the node Q storing the data "0" in the ST 10T SRAM cell is bumped by the read disturbance, NFL is slightly turned ON and the strength of PDL1 is weakened by the increase in VXL through NFL. As a result, the magnitude of the read disturbance increases. On the other hand, the proposed ST 9T SRAM cell avoids this problem by using a cross coupled structure of standard and ST inverters. This is possible because the read disturbance only occurs when storage node Q is "0" in the single BL structure.

A differential writing 10T (10T-P1) SRAM cell has been proposed , which employs a data independent read port to reduce bitline leakage. This cell improves/increases RSNM/read delay and also suffers from low WSNM. We introduce a low standby power 10T (LP10T) SRAM cell with high static noise margins. The main characteristics of the proposed design are as follows: 1. Single-ended structure. 2. Employing separate bitlines to perform read and write operations. 3. Improving read stability using cross-coupled structure of the Schmitt- trigger and standard inverters and separated read path. 4. Performing pseudo differential write operation using write-bitline (WBL) and control signal WWLA. 5. Enhancing write-ability using pseudo differential write operation and write-assist technique. 6. Reducing standby or leakage power consumed by the cell.

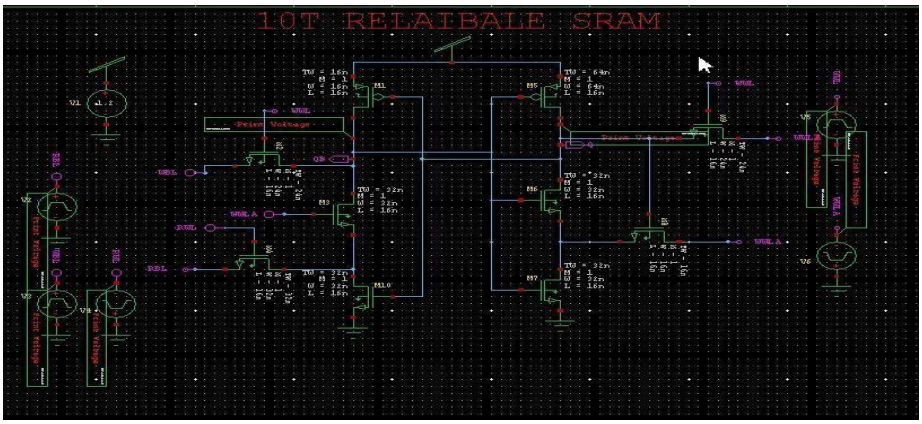
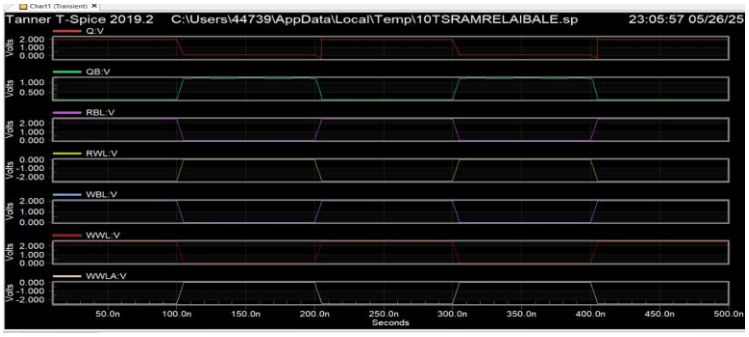
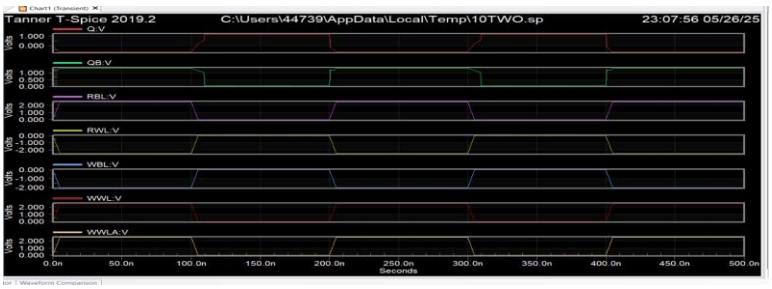
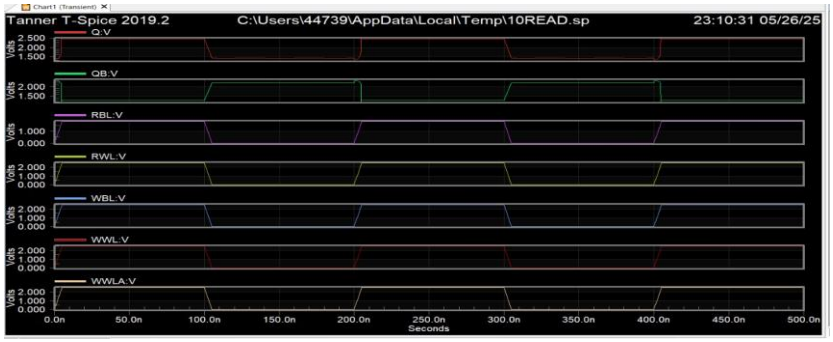
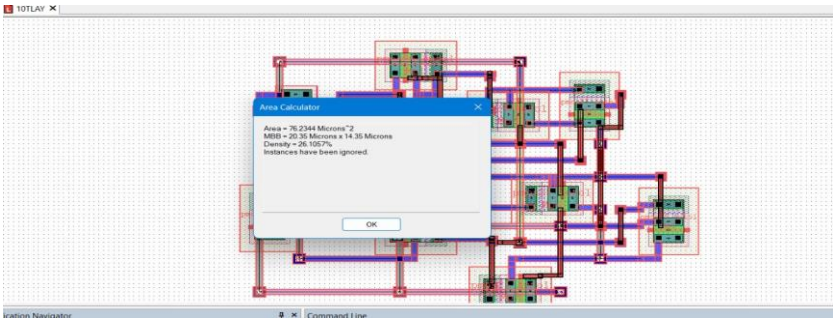



**Figure 6.1.1:** Proposed Method 10T SRAM




This concept was verified using the butterfly curves of the read-disturbance cells. To write new data into the memory, the word-line is activated, and the strong bit-line input-drivers (on top of the schematics) are activated. Depending on the current value stored inside the SRAM cell there might be a short-circuit condition, and the value inside the SRAM cell is literally overwritten. This only works because the transistors inside the SRAM cell are very weak.

## 7-CONCLUSION

In comparison to 12T SRAM, 10T SRAM provides a more efficient and compact solution for memory design. The 10T SRAM cell uses fewer transistors, resulting in reduced silicon area and lower power consumption, which makes it ideal for high-density and low-power applications such as mobile devices and embedded systems. Although 12T SRAM offers

improved read and write stability due to its additional transistors, the 10T design achieves a good balance between stability and efficiency through careful circuit optimization. Overall, 10T SRAM stands out as a cost-effective alternative to 12T SRAM, offering adequate performance while saving space and energy, making it highly suitable for modern VLSI systems.

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