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Designing of Power Efficient CMOS-Based Digital Decoder

Radhika Ravikrindhi, T Pavani, P Pooja

[1]Assistant Professor, Department Of Ece, Bhoj Reddy Engineering College For Women, India.

[2,3]B. Tech Students, Department Of Ece, Bhoj Reddy Engineering College For Women, India.

ABSTRACT

The manuscript delves into the design of digital decoders, specifically focusing on the 4 ×16 and 3 × 8 decoders. It examines the use of 2 × 4 decoders and different logic gates in the design process. Additionally, it explores the implementation of a 4 × 16 decoder using a 3 × 8 decoder and CMOS technology, known for its efficient power usage and fast performance. This study examines power consumption in different architectural configurations, with a specific focus on CMOS-based decoder implementation. The authors adeptly employ Cadence Virtuoso software for circuit realization and evaluation. Power consumption attributes are carefully measured for each decoder design utilizing CMOS technology as the framework. The empirical findings are used as the basis for a thorough comparative analysis, examining the complex connection between circuit architecture and power efficiency. The analysis offers valuable insights for selecting decoders wisely, aiding circuit designers in finding architectures that strike a balance between energy efficiency and uninterrupted operation. Furthermore, it offers a comprehensive insight into power consumption dynamics, contributing to the scholarly community's understanding of energy-efficient digital circuitry. The study has the potential to drive innovation and efficiency in CMOS-based decoding circuits as the field advances.

INTRODUCTION

Power-efficient CMOS-based digital decoders are a critical component in digital electronics, especially in applications requiring low power consumption, such as battery-operated devices, portable systems, and IoT devices. In the critical area of digital decoder design, the optimization of power consumption and performance takes center stage. The study focuses on the intricate architectures of two vital decoder types: the 4 × 16 decoder and the 3 × 8 decoder. These decoders are integral components of digital systems, requiring meticulous design to achieve operational efficiency. The research explores using smaller 2 × 4 decoders as building blocks and investigates various logic gate configurations, offering a modular and hierarchical approach to circuit design. A key aspect of this inquiry is the implementation of a 4 × 16 decoder using a 3 × 8 decoder, demonstrating innovative architectural strategies that improve scalability and adaptability.

2-LITERATURE SURVEY

The design of power-efficient CMOS-based digital decoders has gained significant attention in recent years due to the growing demand for energy- efficient and high-performance digital systems. Digital decoders are widely used in memory address decoding, data routing, and control applications. CMOS technology is favored for its low static power consumption and scalability;

however, dynamic power dissipation caused by frequent switching activity remains a major concern. Researchers have proposed several techniques to reduce power consumption, including transistor sizing, voltage scaling, clock

gating, and the use of pass-transistor logic or transmission gate logic in decoder circuits. Studies have shown that optimized CMOS designs using these techniques can achieve substantial reductions in both dynamic and static power.

Moreover, novel circuit architectures such as dual-threshold CMOS (DTCMOS), adiabatic logic, and reversible logic are being explored to further minimize leakage currents and switching losses. The literature highlights the importance of balancing power efficiency with performance and area constraints, making low-power decoder design a crucial aspect of modern VLSI systems.

2-SOFTWARE REQUIREMENTS

Electronic The group of technologies known as "design automation (EDA) is used to create and develop electronic systems. ECAD (electronic computer-aided design), or just CAD, is what this is. The project's goal is to become familiar with the system's design flow and packaging-level EDA tools, and to validate the tools for proper functioning. The Cadence tool SCM (System Connectivity Manager) is used as an industry standard for System Level designing, Design Entry HDL organizes schematic information into and Cadence PCB Designer provides a scalable, full-featured PCB design solution. The validation is achieved using the generation of test cases, based on either the company's own combination of design steps or based on the CCRs (Cadence Change Requests) filed by the leading customers, which are confidential, since the end product based on the design issues is still to be launched in the market.

The verification based on these issues not only enhances the validation skills, but also provides an insight into the level of complexity at which the System Level Design companies like QUALCOMM, ERICSSON, IBM, CISCO, HP, etc work. Validating the tool not only hones the testing/debugging skills but also greatly improves the design concepts, both in the hardware and the software domains.

The tools are designed and validated for different platforms viz. Linux, Solaris, Windows XP etc. The scripting language Tcl are used for making the test case generation and automation tasks more efficient with respect to time consumption. In this report, significant weightage has been given to understand the design flows of

the Cadence SCM, Cadence Design Entry HDL, and Cadence PCB Designer based on the company's confidential user guides and design workshops.

In this report significant weight age has been given to understand the design flows of the Cadence Part Developer, Cadence Design Entry employs EDA. Large chips are difficult to hand-design. As semiconductor technology continues to scale up, the necessity of EDA for electronics has significantly expanded. Some users include design-service firms that utilize EDA software to evaluate an incoming design's manufacturing readiness and foundry operators that manage semiconductor fabrication facilities, sometimes known as "fabs" or foundries.

EDA Technology

Printed circuit boards (PCBs) and integrated circuits are just two examples of the electronic systems that may be designed and produced using techniques referred to as electronic design automation (EDA). ECAD (electronic computer-aided design) or plain CAD are other names for this. Specialized talks on the EDA used for printed circuit boards and wire wrap are both present. To create and analyze complete semiconductor devices, chip designers employ a set of interconnected tools known as a design flow.

The objective of the project is to learn the design flow of System and Packaging level EDA tools, and to validate the tools for proper functioning. Allegro Design Workbench (ADW) represents a suite of products that help implement a collaborative design

environment involving your design teams, methodologies, corporate design databases, and tools. In addition, you can use design lifecycle, library development and management, and data management features to control the design and library management processes.

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Some users include design-service firms that utilize EDA software to evaluate an incoming design's manufacturing readiness and foundry operators that manage semiconductor fabrication facilities, sometimes known as "fabs " or foundries. Using a computer to design, lay out, check, and simulate the operation of electronic circuits on a chip or printed circuit board is known as electronic design automation. While the general audience is only slightly aware of the chips and circuitry inside and primarily concentrates on the finished products. With the ongoing growth of semiconductor technology, EDA for electronics has significantly grown in relevance. Programming design functionality into FPGAs also uses EDA tools.

3-DIGITAL DECODER

In modern digital systems, CMOS-based decoders are fundamental components used for address decoding, data routing, and control signal generation. The existing decoder designs, built using conventional CMOS logic, offer advantages such as low static power consumption and high noise immunity. However, as technology continues to scale down and devices become more compact and power-sensitive, these traditional decoders face significant challenges. Notably, they suffer from increased dynamic power consumption due to frequent switching activities and higher leakage currents, particularly in submicron technologies. This leads to inefficiencies in power-critical applications such as portable electronics, IoT devices, and embedded systems.

To address these issues, the proposed system introduces a power-efficient CMOS-based digital decoder design that focuses on optimizing power usage without compromising functionality. The proposed approach incorporates advanced low-power techniques such as power gating using sleep transistors, transistor sizing optimization, and logic minimization strategies to reduce both dynamic and static power dissipation. By integrating these methods, the proposed decoder aims to achieve substantial improvements in energy efficiency, making it more suitable for modern low-power digital applications.

Decoders

A decoder is a combinational logic circuit that

converts a binary code into a unique output, activating one of multiple output lines based on the input. Types of decoders include binary decoders, BCD decoders, priority decoders, address decoders, and seven-segment decoders.

Types of Decoders

1. **Digital Logic Decoders**

Digital logic decoders are essential combinational circuits used in digital electronics to convert coded binary inputs into specific output signals. They are crucial in applications like memory addressing, data demultiplexing, display driving, and control logic. A decoder typically has n input lines and 2^n output lines, where only one output is activated (usually set to logic '1') based on the binary input combination.

- 2-to-4 Decoder – 2 inputs, 4 outputs.
- 3-to-8 Decoder (e.g., 74HC138 IC) – 3 inputs, 8 outputs (with enable control).
- 4-to-16 Decoder – Expands using multiple 3-to-8 decoders.

2. **BCD-to-Decimal Decoders**

BCD-to-Decimal decoders are specialized combinational logic circuits designed to convert a 4-bit Binary-Coded Decimal (BCD) input into one of ten corresponding decimal digit outputs (0 through 9). These decoders play a crucial role in digital systems where numerical data must be processed or displayed in human-readable form.

- 7442 IC – Ignores invalid BCD inputs (1010 to 1111).
- Active-Low vs. Active-High – Determines output logic (e.g., 7442 is active-low).

3. **BCD-to-7-Segment Decoders**

A BCD-to-7-segment decoder is a digital circuit or IC (integrated circuit) that converts a Binary Coded Decimal (BCD) input into control signals to drive a 7- segment display. These displays are commonly used to represent decimal numbers (0–9) in devices like digital clocks, calculators, and counters.

4-RESULTS AND DISCUSSION

In modern low-power digital systems, minimizing energy consumption is critical, particularly in portable and battery-operated devices. This project aimed to develop a 3-to-8 line digital decoder using complementary metal-oxide- semiconductor (CMOS) logic, with emphasis on reducing dynamic and static power dissipation. The design process incorporated various power-saving techniques, including transistor sizing optimization, logic minimization, and leakage reduction strategies.

2×4 Decoder Simulation Result

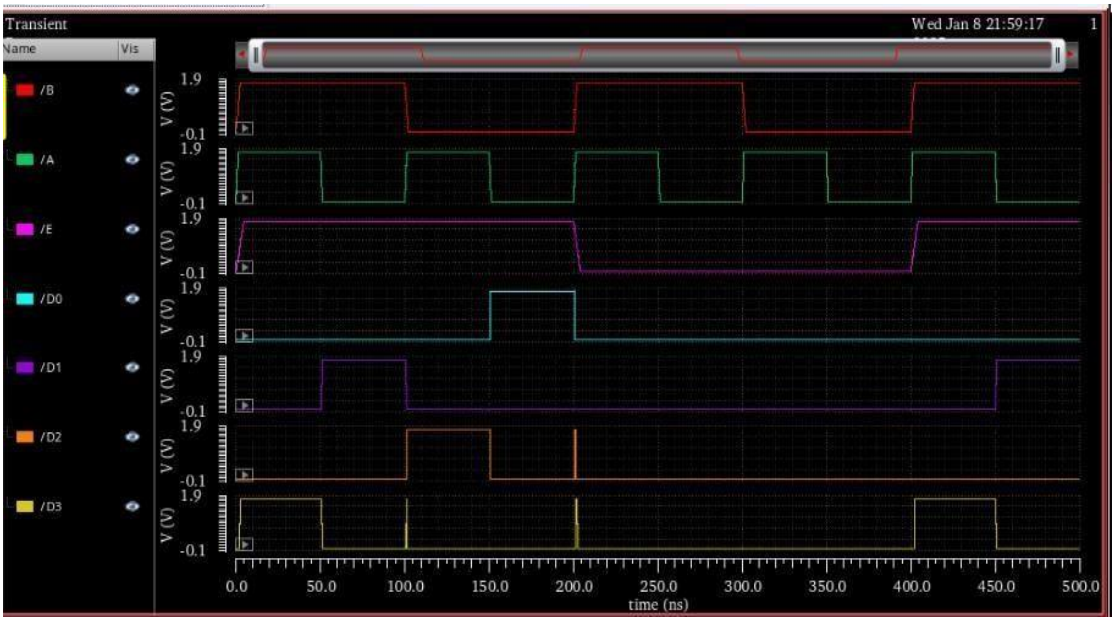

Fig.1: Simulation of 2x4 decoder with enable pin

A 2-to-4 line decoder is a fundamental combinational circuit that takes two binary input signals and activates exactly one of its four output lines based on the binary value of the inputs. The decoder has two inputs, commonly labeled A1 and A0, and four outputs, Y0 through Y3. Each output corresponds to one unique combination of the input signals, ensuring that only one output is asserted high at any time while the others remain low. Specifically, when the inputs are 00, the output Y0 is activated; for inputs 01, Y1 is activated; for 10, Y2 is active; and for 11, Y3 is activated. This behavior is described by simple logic expressions where each output is generated

by combining the inputs and their complements using AND gates. For instance, Y0 is produced by the logical AND of NOT A1 and NOT A0, and similarly for the other outputs. The 2×4 decoder is essential in digital systems for address decoding, data routing, and control signal generation, providing a clear, one-hot output representation of the input binary code.

- Enable Signal (EN):
  - If EN = 0, all outputs are forced to 0, regardless of A and B.
  - If EN = 1, the decoder operates normally.
- Binary Inputs (A and B):
  - The binary inputs A and B determine which AND gate is activated.
  - For example:
  - A=0, B=0A = 0, B = 0A=0, B=0: Only Y0Y_0Y0 is HIGH.
  - A=0, B=1A = 0, B = 1A=0, B=1: Only Y1Y_1Y1 is HIGH.
  - A=1, B=0A = 1, B = 0A=1, B=0: Only Y2Y_2Y2 is HIGH.
  - A=1, B=1A = 1, B = 1A=1, B=1: Only Y3Y_3Y3 is HIGH.
- Output Activation:
  - The combination of A, B, and EN activates only one AND gate, setting the corresponding output HIGH while all others remain LOW.

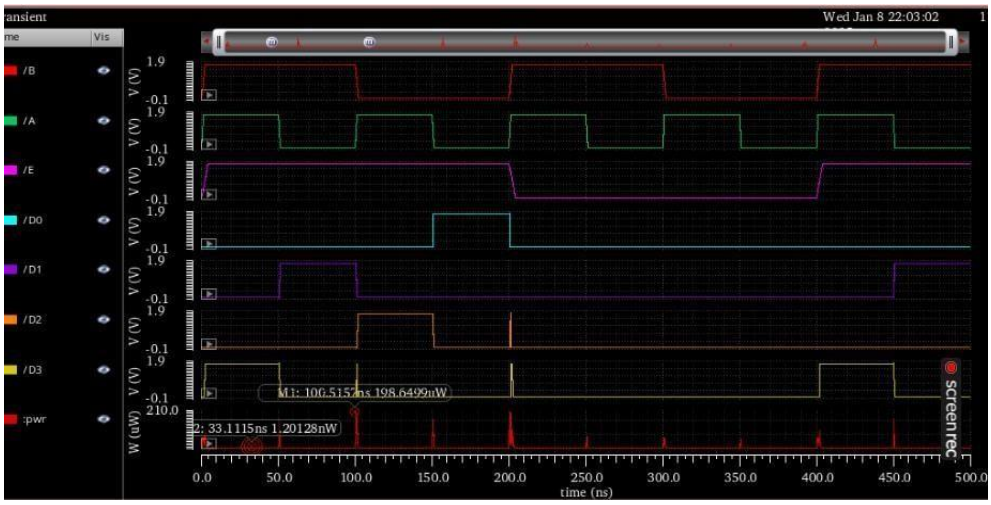

Fig.2: Power Analysis of 2x4 decoder with enable pin

A 2-to-4 line decoder is a combinational logic circuit that decodes a 2-bit binary input into one of four unique outputs. It has two input lines (A and B) and four output lines (Y0 to Y3). Each output corresponds to one of the possible combinations of the input bits. An enable input (EN) is often included to control whether the decoder is active.

Working Principle:

- Inputs: Two binary inputs, A and B, and an enable input, EN.
- Outputs: Four outputs, Y0, Y1, Y2, and Y3.

When the enable input (EN) is high (logic level 1), the decoder operates normally. The outputs are determined by the combination of inputs A and B:

- If A = 0 and B = 0, then Y0 is high (1), and Y1, Y2, Y3 are low (0).
- If A = 0 and B = 1, then Y1 is high, and Y0, Y2, Y3 are low.
- If A = 1 and B = 0, then Y2 is high, and Y0, Y1, Y3 are low.
- If A = 1 and B = 1, then Y3 is high, and Y0, Y1, Y2 are low.

When the enable input (EN) is low (logic level 0), all outputs are forced to low, regardless of the inputs A and B. This allows the decoder to be effectively turned off when not needed.

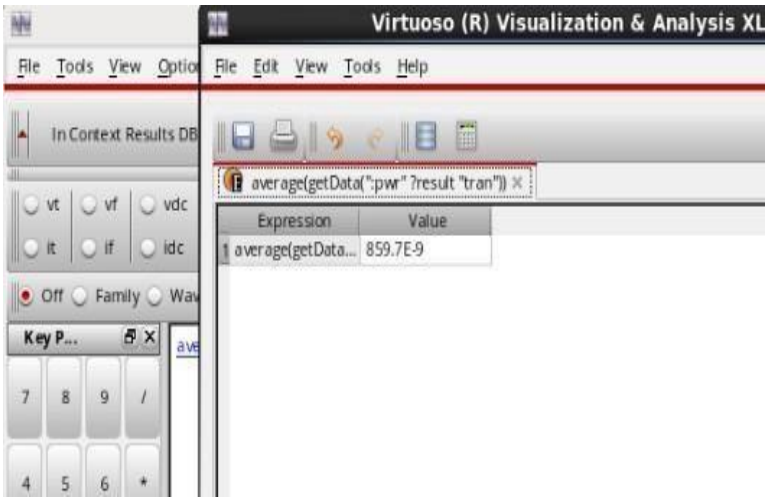

Fig.3: Average Power Analysis of 2x4 decoder with enable pin

3

×8 Decoder Simulation Result

The 3-to-8 line decoder is a combinational logic

circuit that accepts three binary input signals and activates exactly one of its eight output lines according to the binary value represented by the inputs. The inputs are usually labeled A2, A1, and A0, and the outputs range from Y0 to Y7. Each output corresponds to a unique combination of the input signals, such that only one output line is high (logic 1) at a time while all others remain low (logic 0). For example, when the inputs are 000, output Y0 is enabled; when the inputs are 001, output Y1 is enabled; and so on, up to input 111 which activates output Y7.

This decoding function is typically realized through AND gates combined with the appropriate input signals and their complements, following the logical expressions where each output is the AND of the three inputs in either true or complemented form. The 3×8 decoder is widely used in digital systems for address decoding, multiplexing, and control signal generation, providing an efficient means of converting binary information into a one-hot output code.

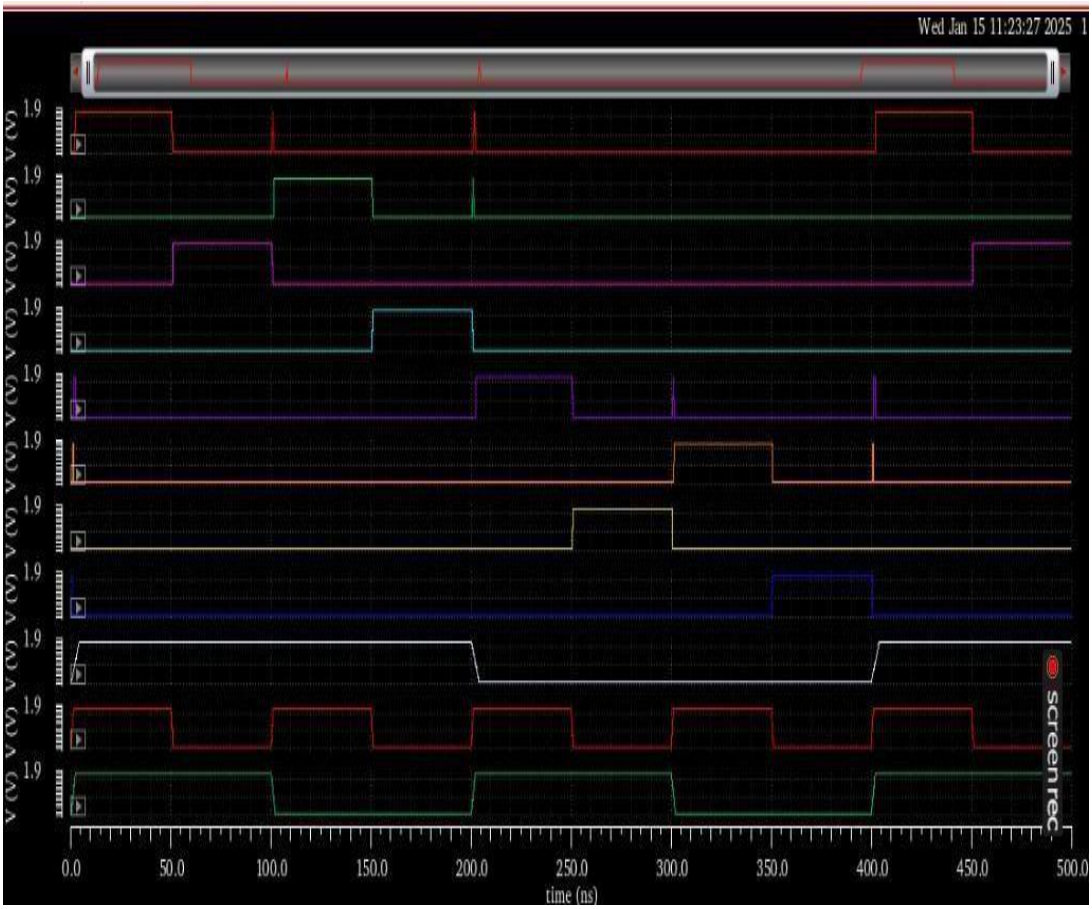

Fig.4: Simulation of 3x8 decoder with enable pin

The power consumption of a 3×8 digital decoder implemented in CMOS technology is mainly influenced by two components: dynamic and static power. Dynamic power is associated with the switching of internal nodes and output lines as the input changes, leading to energy loss due to charging and discharging of capacitances. Since only

one output is active at a time, the overall switching activity is relatively moderate but still depends on input frequency and load conditions.

Static power, meanwhile, is caused by leakage currents present even when the circuit is idle, and it becomes more prominent in advanced technology nodes with smaller transistors. In addition, short bursts of power loss can occur during transitions when both pull-up and pull-down networks momentarily conduct, contributing to short-circuit power. Effective power optimization involves reducing switching activity, careful circuit design, and adopting power-saving techniques such as clock gating or using high-threshold devices in non-critical paths. Overall, the total power usage of a 3×8 decoder is a function of its design style, operating conditions, and fabrication technology.

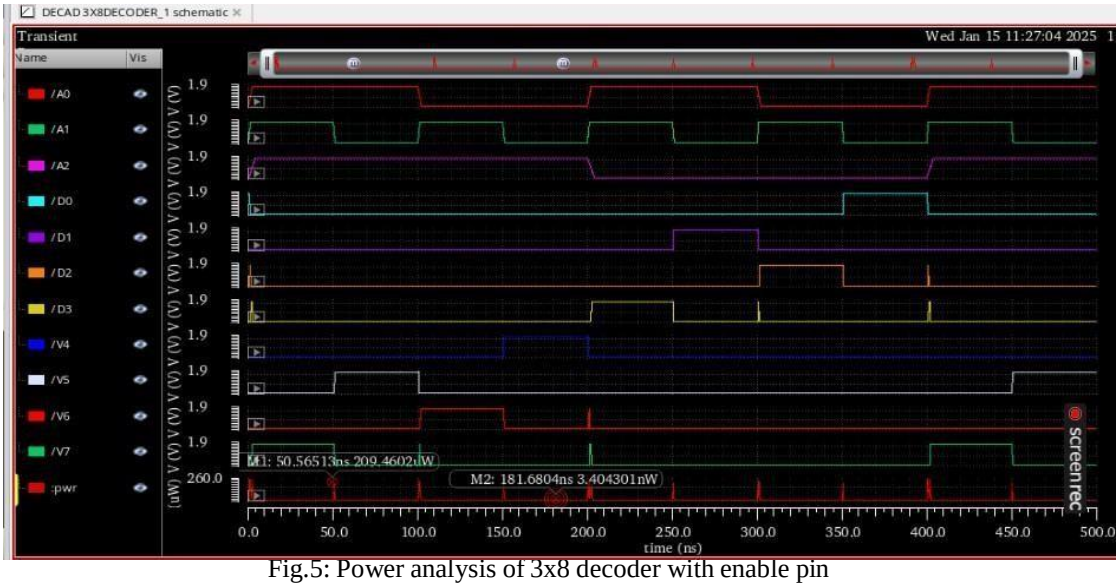

Fig.5: Power analysis of 3x8 decoder with enable pin

5-CONCLUSION

Here, we explored decoder design and examined its complex aspects. We have discovered valuable characteristics that will advance this critical field through careful implementation and analysis. Decoder configurations are thoroughly studied for power consumption and efficiency. The crux of our findings lies in the power analysis conducted for each decoder configuration. The 4 × 16 decoder with 2 × 4 decoders is known for its high power consumption due to its hierarchical structure and the cascading effect of multiple decoding layers.

The 3 × 8 decoder with 2 × 4 decoders is a more efficient option, as it uses a composite decoding approach that balances complexity and energy conservation. The individual 2 × 4 decoder showcases efficient energy utilization, highlighting the beauty of simplicity in circuit design. The 4 × 16 decoder, implemented using 3 × 8 decoders, strikes a balance between complexity and energy efficiency. This study connects theory and experiment, making conceptual knowledge applicable. The insights gathered here have the potential to spark innovation in power-efficient decoder design. The potential impact of digital circuitry, particularly CMOS-based decoding circuits, is anticipated to have a ripple effect.

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