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A DFT Compatible In-Situ Timing Error Detection and Correction Structure

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ABSTRACT

In-situ timing error detection and correction (EDAC) structure is widely adopted in timing-error resilient circuits to reduce the conservative timing guard-band induced by process, voltage, and temperature (PVT) variations. However, it introduces the latch-based data-path as well as extra detection and propagation logic, therefore challenges the design for-testability (DFT) implementation. In this article, we propose a novel DFTcompatible EDAC structure with significant signal control simplification and test- pattern complexity reduction, featuring low area and test overhead. This structure leverages a new scannable EDAC cell (SEDC) which can be configured for timing EDAC in normal mode, or for shift operations as a flip-flop in scan mode. Specifically, the proposed detection logic can be controlled succinctly in scan shift operations and then observed via the global error propagation logic with simple control signal configurations during the test.

The performance of the full adder would impact the whole system. Full Adder Cell plays an important role in Digital Signal Processors (DSPs), Application Specific ICs (ASICs), and microprocessors, etc. Fault categorized into three categories permanent, transient or intermittent. Due to the presence of electromagnetic noises, cosmic rays, crosstalk and power supply noises, transient fault takes place. The system leads to failure and when the faults exist on a system than stop delivering the desired results. In the practical system, it is impossible to create a perfect system, so fault tolerant is essential. When faults are present in a system and system is capable of performing its desired function continuously that's called the fault tolerant. Fault- tolerant design is used to attain a reliability or availability which cannot be obtained by its counterpart the faultintolerant design.

1 INTRODUCTION

An adder is a basic digital circuit with which we can perform addition of numbers, and it is a very fundamental building block of the Arithmetic Logic Unit (ALU). It is used in many computers and different kinds of processors. The adder is one of the most vital components of a processor. The performance of the full adder would impact the whole system. Full Adder Cell plays an important role in Digital Signal Processors (DSPs), Application Specific ICs (ASICs), and microprocessors, etc. Fault categorized into three categories permanent, transient or intermittent. Due to the presence of electromagnetic noises, cosmic rays, crosstalk and power supply noises, transient fault takes place. The problem created by that kind of fault is that it's not easy to an identified specific faulty full adder, so we have to replace the complete adder whenever an error is found.

The system leads to failure and when the faults exist on a system than stop delivering the desired results. In the practical system, it is impossible to create a perfect system, so fault tolerant is essential. When faults are present in a system and system is capable

of performing its desired function continuously that's called the fault tolerant. Fault-tolerant design is used to attain a reliability or availability which cannot be obtained by its counterpart the fault-intolerant design.

Fault-tolerance techniques increase the cost of redundancy in computer systems that are the only bottleneck in its use. Computing systems that need high performance are highly susceptible to permanent faults and transient errors. Fault tolerance would be the only technology for building commercial systems when performance demand increases. Fault tolerance would remain a vital attribute for systems required in safety, business, and mission-critical applications. We have to deal with the problem that is considered above so we introduced self-checking and self-repairing fault tolerant full adder. The faults that make full adder cell faulty are classified into two categories single faults and the double faults. Double fault very typical to recognize which makes both the output faulty and hard to repair as compared to the single fault which makes only one output faulty and also makes system more complicated and high area overhead requirement. If we want to make the fault-tolerant full adder, lesser area overhead plays an important role, an increased area overhead result in an increased transistor count which increases system complexity. The aim of the fault-tolerant design is to diminish the probability of failures. In the literature, many techniques have been used by the researcher such as hardware redundancy and time redundancy.

2- LITERATURE SURVEY

As modern integrated circuits (ICs) continue to scale towards smaller process nodes and higher operating frequencies, they become increasingly vulnerable to timing errors caused by process variations, voltage fluctuations, temperature shifts, and aging effects. Ensuring timing correctness across all corners without excessive timing margins is a significant challenge in digital design.

The objective of this literature survey is not merely to summarize previous work, but to critically evaluate its strengths and weaknesses, highlight emerging trends, and pinpoint areas where further research is warranted. Specifically, in the context of timing error management, the review will delve into different categories of timing detectors (e.g., razor flip-flops, error-detection latches, custom delay sensors), their respective principles of operation, performance overheads, and practical limitations. It will also explore various proposed adaptive correction mechanisms, such as dynamic voltage and frequency scaling (DVFS), pipeline flushing, and re-execution strategies, assessing their effectiveness and applicability to fine-grained timing errors.

Furthermore, the survey will critically analyze existing DFT strategies, particularly those related to real-time monitoring and adaptive circuits, to understand how the proposed in-situ solution can seamlessly integrate with and leverage established test infrastructures. By identifying the specific technical challenges that remain unaddressed by current solutions, this literature review will clearly delineate the scope for the novel contributions presented in this thesis, establishing the research's originality and significance within the broader field of reliable VLSI design.

Design and Analysis of Low-power 10-Transistor Full Adder Using Novel Xor-Xnor Gates

Full adders are important components in applications such as digital signal processors (DSP) architectures and microprocessors. In this paper, we propose a technique to build a total of 41 new 10-transistor full adders using novel XOR and XNOR gates in combination with existing ones. We have done over 10,000 HSPICE simulation runs of all the different

adders in different input patterns, frequencies, and load capacitances. Almost all those new adders consume less power in high frequencies, while three new adders consistently consume on average 10% less power and have higher speed compared with the previous 10-transistor full adder and the conventional 28-transistor CMOS adder. One drawback of the new adders is the threshold-voltage loss of the pass transistors.

Conventional full adder designs often use 28 transistors, leading to increased power consumption and area. Recent research focuses on reducing transistor count and power consumption while maintaining performance. XOR-XNOR gates are essential components in full adder design, enabling efficient implementation of complex logic functions.

Analysis of Various Full-Adder Circuits In Cadence

The Adder is the important part in any processor/controller design. Till date there are a plenty of 1-bit full-adder circuits which have been proposed and designed. In this paper we have a analytic and comparative description of various full adder circuits, considering various constraints like power consumption, speed of operation and area. The circuits are designed in the virtuoso platform, using cadence tool with the available GPDK - 45nm kit. The Full adder circuits with the most 28 transistors to the one with only 6 transistors are successfully designed, simulated and compared for various parameters like power consumption, speed of operation(delay) and area (transistor count), and finally concluded the best designs, that suite for the particular specifications.

The design and analysis of full-adder circuits are crucial in digital electronics, as they form the backbone of arithmetic logic units (ALUs) and other digital systems. In this analysis, we explore various full-adder circuits implemented in Cadence, a popular electronic design automation (EDA) tool. Our investigation focuses on the performance, power consumption, and area efficiency of different full-adder designs.

The conventional full adder is a basic digital circuit that performs binary addition. It consists of 28 transistors and uses a complementary metal-oxide-semiconductor (CMOS) logic style. Our analysis in Cadence reveals that the conventional full adder exhibits reliable performance, but its power consumption and area are relatively high compared to other designs.

To address the power consumption issue, various low-power full adder designs have been proposed. One such design uses a 10-transistor architecture with XOR-XNOR gates. Our Cadence simulations show that this design achieves significant power reduction while maintaining comparable performance to the conventional full adder. Another design uses a hybrid logic style, combining CMOS and pass-transistor logic (PTL) to reduce power consumption and area.

We compared the performance of different full-adder circuits in Cadence, focusing on parameters such as propagation delay, power consumption, and power-delay product (PDP). Our results indicate that the 10-transistor full adder design with XOR-XNOR gates exhibits the best PDP, making it suitable for low-power applications. However, the conventional full adder shows better performance in terms of propagation delay.

3-TECHNOLOGIES

However, integrating TEDC mechanisms with standard design-for-testability (DFT) methodologies remains a challenge. Traditional TEDC structures often interfere with scan chains or require custom design flows, complicating their adoption in commercial design environments. Therefore, a DFT-

compatible in-situ timing error detection and correction structure is essential to ensure seamless integration into existing test infrastructures without sacrificing error coverage or system performance.

Technologies Used (EDM)

Tanner EDA is unrivalled in the field of integrated circuit (IC) design. Physical layout, design rule checks (DRC), layout versus schematic (LVS) checks, schematic capture, SPICE simulation, and many more phases may all benefit from it. The main tools are S-Edit is one such tool; it's used for making and documenting circuit diagrams. To model the operation of electronic circuits, one may utilize T-SPICE, a SPICE-based simulation engine that is compatible with S-Edit. Chip layouts may be made with the use of LEdit, a physical design tool.

Using S-Edit and T-SPICE

S-Edit allows you to create schematic diagrams of circuits, which can later be used to generate the physical layout of an integrated circuit. Additionally, S-Edit integrates with TSPICE, which enables you to perform detailed SPICE simulations of your circuits directly from within the S-Edit environment.

One example of using these tools would be to simulate the behaviour of an NMOS transistor. In S-Edit, you can document the circuit schematic and then use T-SPICE to simulate the transistor's characteristics, such as current-voltage (I-V) curves.

Initial Setup and Library Download

Get on a computer at the sixth level of the Cob Leigh building. This will be your directories.Arrange all of your Tanner EDA projects in a directory. Making a folder called EELE414_VLSI_Fall2011/Tanner_Projects is one example.

Get the libraries: o Get the Tanner Libraries.zip file from the course website. Then, unzip it. Place the contents of the archived file into the Tanner_Projects folder. Circuit symbols, SPICE models for simulation, and definitions for physical layout, DRC, and LVS checks are all part of the files that make up this zip bundle and are essential for your S-Edit designs.

With this configuration, you can be confident that Tanner EDA tools have all the models and libraries you need to build circuits, conduct simulations, and verify layouts.

To begin working with S-Edit and T-SPICE, the initial setup involves installing the software and configuring the environment. This includes downloading and installing the necessary libraries and components. The library download process typically involves accessing the official repository or website, selecting the required libraries, and following the installation instructions. Once the libraries are installed, users can access a wide range of components and models, enabling them to design and simulate complex electronic circuits. Proper setup and library management are crucial for ensuring accurate simulation results and efficient design workflow. By completing the initial setup and library download, users can leverage the full capabilities of S-Edit and T-SPICE for their electronic design and simulation needs.

4-DESIGN AND IMPLEMENTATION

With the continuous scaling of semiconductor technology, modern integrated circuits (ICs) face increasing challenges in maintaining timing reliability. Variations in process parameters, supply voltage fluctuations, temperature changes, and device aging can all contribute to timing errors, potentially leading to performance degradation or functional failures. Traditional design approaches address these concerns by incorporating large timing margins, but this often results in increased power consumption and reduced performance efficiency.

Working Principle of EDAC Structure

EDAC structure reduces the pessimistic timing guradbands through *in-situ* detection of possible timing violations with specific EDAC cells and propagation logic. As exemplified in the bottom of the first five pipeline stages (IF, DE, RA, EX, and MEM) were protected in a timingerror resilient processor, where 12% FFs at the endpoints of critical paths were replaced by the EDAC cells. The top of Fig. 1 shows the EDAC cell structure and its conceptual timing diagram. As shown in the diagram, if the input data (*D*) arrived late due to variation, the detection logic (XOR gate) would generate an error signal (error). Specifically, a positive latch was adopted in the data path due to its metastability immunity and time- borrowing ability.

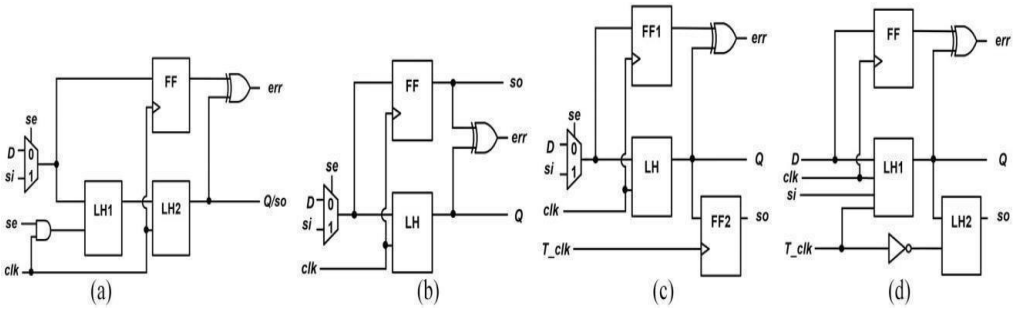

Fig 4.1: Structures of previous scannable EDAC cells: (a) Extra-latch-added scannable error detection cell (b) SSFF (c) STFF and (d) level-sensitive scan design-based cell (LSSD-based cell)

Then, the local error signals from each cell in the pipeline were collected by the propagation logic (OR tree) to generate the pipeline-error signal (e.g., errorDE in the DE stage). This error signal was pipelined to error control. Considering the variation happens infrequently, the energy saved by guard band mitigation overwhelms the overhead of EDAC, which enables a better performance-energy trade-off.

The EDAC structure works by adding redundant bits to the original data, enabling detection and correction of errors. When data is transmitted or stored, EDAC encodes it with additional parity bits. Upon retrieval or reception, the EDAC decoder checks for errors by recalculating the parity bits. If an error is detected, EDAC can correct single-bit errors or detect multi-bit errors, ensuring data integrity and reliability. This process involves encoding, transmission/storage, decoding, error detection, and correction, providing a robust mechanism for maintaining data accuracy.

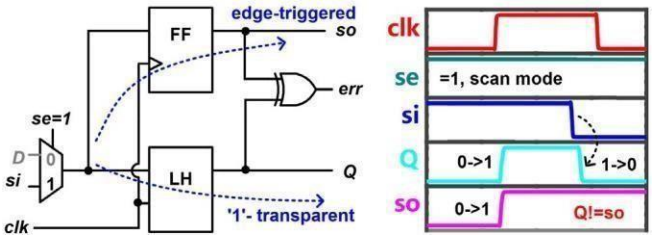

Fig 4.2: Illustration of inconsistency between *so* and *Q* in SSFF in a scan shift Operation

Previous Test Methods For EDAC Structure

Based on the presented EDAC cells, how to test error DP logic has been previously discussed in Yuan prepared the individual long path delay pat- terns to ensure only the detection logic in the targeted EDAC cell can be activated, then tightened the clock period

pro-gressively to generate timing error at this cell. To evaluate the faults, it compared the captured data with golden values assisted by the OR tree output to check whether the targeted local error was generated and captured successfully. Based on utilized the binary search to accelerate the process of finding the proper clock configurations for error generation.

5-SIMULATION RESULTS

To overcome these limitations, **in-situ timing error detection and correction (TEDC) techniques** have been introduced. These techniques dynamically monitor circuit timing during operation, detecting and mitigating errors as they occur. By enabling adaptive correction mechanisms, TEDC structures allow circuits to operate closer to their performance limits while improving energy efficiency and reliability.

However, integrating TEDC structures into conventional **Design-for-Testability (DFT)** methodologies presents significant challenges. Traditional DFT techniques, such as scan-based testing, primarily target stuck-at and transition faults but do not account for dynamic timing failures occurring in real-time operation. Additionally, incorporating TEDC structures into existing test flows may introduce design overhead, complicating testability and validation.

Inverter Schematic

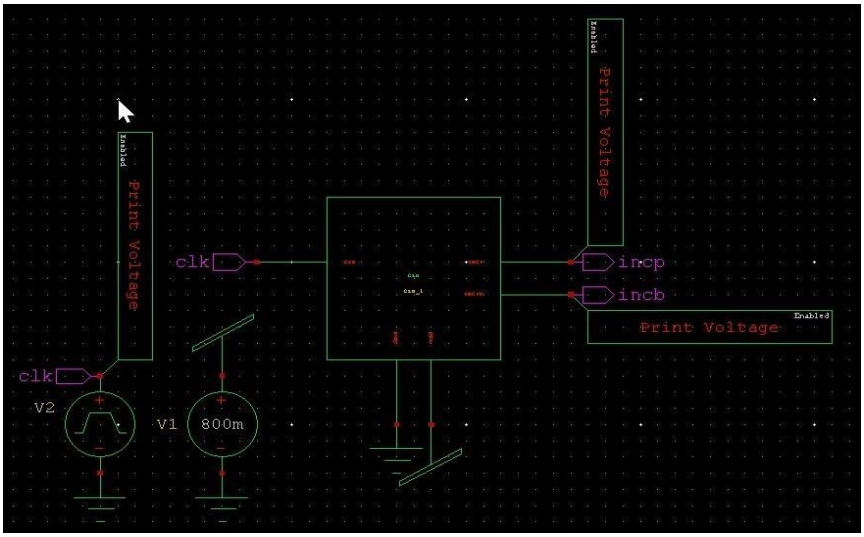

Fig 5.1: Schematic for clock

A CMOS inverter is a fundamental building block of digital circuits, particularly in logic gates and microprocessors. It consists of a p-channel MOSFET (PMOS) and an n-channel MOSFET (NMOS) connected in a complementary configuration.

The method, in which the low voltage DC power is inverted, is completed in two steps. The first step is the conversion of the low voltage DC power to a high voltage DC source, and the second step is the conversion of the high DC source to an AC waveform using pulse width modulation. Another method to complete the desired outcome would be to first convert the low voltage DC power to AC, and then use a transformer to boost the voltage to 120/220 volts. The widely used method in the current residential inverter is the second one and hence this reference design is based on this method.The AC input is sensed through isolated amplifier (AMC1100) and the isolated replica of the AC input is given to the TI's Picolo Lite Microcontroller ADC. When the AC input is not present in Valid range (Inverter mode) or AC fails, the relay between Mains AC Input and the Inverter Output remain open, the microcontroller generates PWMs and send four

drives output to Gate Driver (SM72295). Now the Gate Driver accepts low-power inputs from the controller and produces the appropriate high-current gate drive for the power MOSFETs placed in Full Bridge Topology. Here H-bridge circuit converts battery DC voltage into AC using high frequency PWM (6 kHz to 20 KHz) thus feeding the 50-Hz transformer which Boost it to 120V/220V AC. The output of transformer contains a capacitor which filters it to make clean 50-Hz AC.

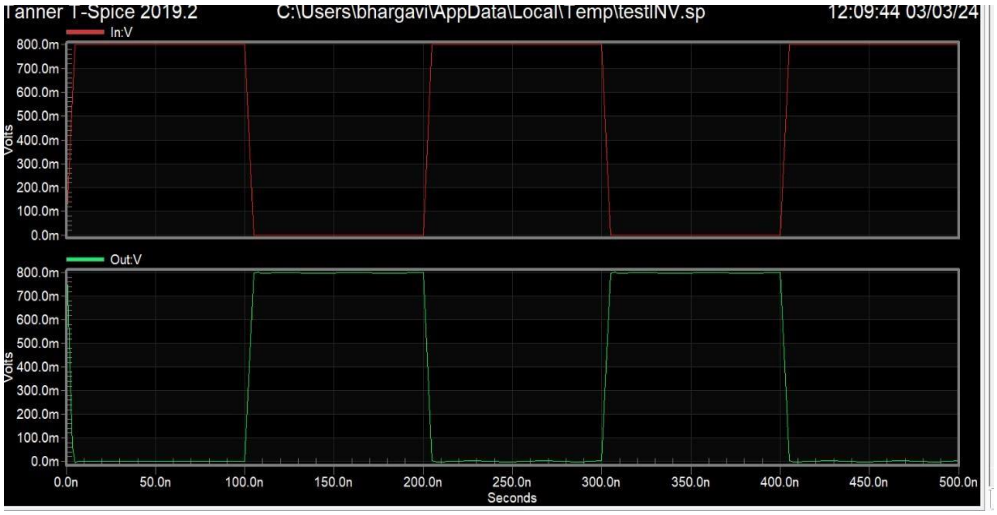

Fig 5.2: Simulation results of clock

Structure of a CMOS Inverter

• The NMOS transistor is connected to ground (GND)**.**

• The PMOS transistor is connected to Vdd (supply voltage)**.**

• The input (Vin**)** is applied to the gates of both transistors.

• The output (Vout) is taken from the common drain connection of NMOS and PMOS.

The CMOS inverter is crucial in electronics, employed in memory chips and microprocessors among others. It generates complementary outputs whenever there are input signals through it. These inverters allow flexibility among circuit designers because they can be classified into many categories depending on their abilities and arrangements.For their functionality, NMOS and PMOS transistors should counteract each other whereby they may react to input voltages by oscillating between conductive and non-conductive modes. Silicon substrates are host to connecting metal layers, transistors, and resistors in CMOS inverter components.

In order to create a CMOS inverter, one has to merge two types of transistors : PMOS and NMOS respectively.The process requires that you connect them in this way, thus, there must be one NMOS and one PMOS transistor consisting a CMOS inverter made on the same silicon chip.The input terminal is made up of NMOS and PMOS transistors that have an input voltage applied to their gates together with an output terminal which is connected to drains of the two transistors.

The sources of PMOS and NMOS transistors are attached to distinct power supply voltages unlike in the case of the other terminals. Specifically speaking, the NMOS transistor is connected to ground (0 V) while its counterpart, PMOS transistor is connected to a positive power supply voltage (Vdd).

The diagram is shown with two transistors tied up in series between the ground and the power source in it.Unlike PMOS transistors where the source is linked to power supply and the drain is tied to the output , an NMOS transistor’s source is directly linked with earth while its drain is linked with output

.The input to the inverter is actually a mutual connection between the gates of the two transistors.When the input level reaches logic level 0, the NMOS transistor is on which causes PMOS transistor to be cut-off therefore causing high output. On the contrary, in a scenario where NMOS transistor goes off, inverter's output is low due to high input voltage.

As exemplified in Fig. we assume an EDAC-based circuit contains five scannable sequential cells, including two SEDCs and a one-stage OR tree, whose output is captured by the final FF without loss of generality. The signal names and descriptions are summarized. These sequential cells excluding the final FF make up one chain clocked by *clk* in the scan mode. The final FF is configured for the error-propagation logic observation. As discussed in the previous section, error signals might be flagged at the high clock phase in normal mode or the low clock phase in scan mode, so the final FF can be triggered by different clock edges depending on the operation modes. Besides, we introduce a new control signal, *seot*, to select the input data of the final FF.

Voltage Transfer Characteristics (VTC)

The Voltage Transfer Characteristics (VTC) describe how the output voltage changes with respect to the input voltage. The main regions are:

• Region 1 (Low Input, High Output): When Vin is low, the PMOS is fully ON, and NMOS is OFF.

• Region 2 (Transition Region): Both transistors are partially conducting, leading to a rapid voltage change.

• Region 3 (High Input, Low Output): When Vin is high, NMOS is fully ON, and PMOS is OFF.

The switching threshold Vth is the voltage at which both transistors conduct equally.

Region-1 : In this region the input is in the range of (0,Vtn). Since the input voltage is less than Vtn, the NMOS is in cutoff region. No current flows from Vdd to Vss, The entire Vdd will appear at the Output terminal.

NMOS is in cutoff as Vgs < Vtn

PMOS is in linear as Vgsp < Vtp and Vdsp > Vgsp - Vtp.

Zero current flows from supply voltage and the power dissipation is zero.

Region-2 : In this region the input is in the range of (Vtn,Vdd/2). Since the input voltage is greater than Vtn the NMOS is conducting and it jumps to saturation as it has large Vds across it(Vout is high). PMOS still remains in the linear region.

NMOS is in saturation as Vgs > Vtn and Vout >Vin - Vtn.

PMOS is in linear region as Vdsp > Vgsp -Vtp.

since both the transistors are conducting some amount of current flows from supply in this region.

Region-3 : In this region the input voltage is Vdd/2. At this point the output voltage is also Vdd/2 as one can see in figure-2. At this voltage both the NMOS and PMOS are in saturation and the output drops drastically from Vdd to Vdd/2. At this point a large amount of current flows from the supply. Most of the power consumed in CMOS inverter is at this point. So care should be taken that the Input should not stay at Vdd/2 for more amount of time.

NMOS is in saturation as Vgs > Vtn and Vout >Vin - Vtn.

PMOS is in saturation as Vgsp < Vtp and Vdsp < Vgsp -Vtp.

Large amount of current is drawn from supply and hence large power dissipation.

Region-4 : In this region the input voltage is in the range of (Vdd/2 , Vdd-Vtp). Here the PMOS remains in saturation as Vout < Vin - Vtp and Vgsp < Vtp. But the NMOS moves from saturation to linear region since the drain to source voltage now is less than Vgsn-Vtn.

NMOS is in linear as Vgs > Vtn and Vout < Vin - Vtn.

PMOS is in saturation as Vgsp < Vtp and Vdsp < Vgsp -Vtp.

A medium amount of current is drawn as NMOS is in linear region and power dissipation is low.

Region-5 : In this region the input voltage is in the range of (Vdd-Vtp,Vdd). Here the PMOS moves from saturation to cutoff as the Vgsp is so high that Vgsp > Vtp. The NMOS still remains in linear as the drain to source voltage now is less than Vgsn-Vtn.

NMOS is in linear as Vgs > Vtn and Vout < Vin - Vtn.

PMOS is in cutoff as Vgsp > Vtp.

Zero current flows from the supply and so the power dissipation is zero.Now that we have clearly understood the voltage transfer characteristics and operation of an NMOS, we will discuss how to alter the transfer characteristics of any CMOS gate in the next article.

5.3 2X1 Multiplexer:

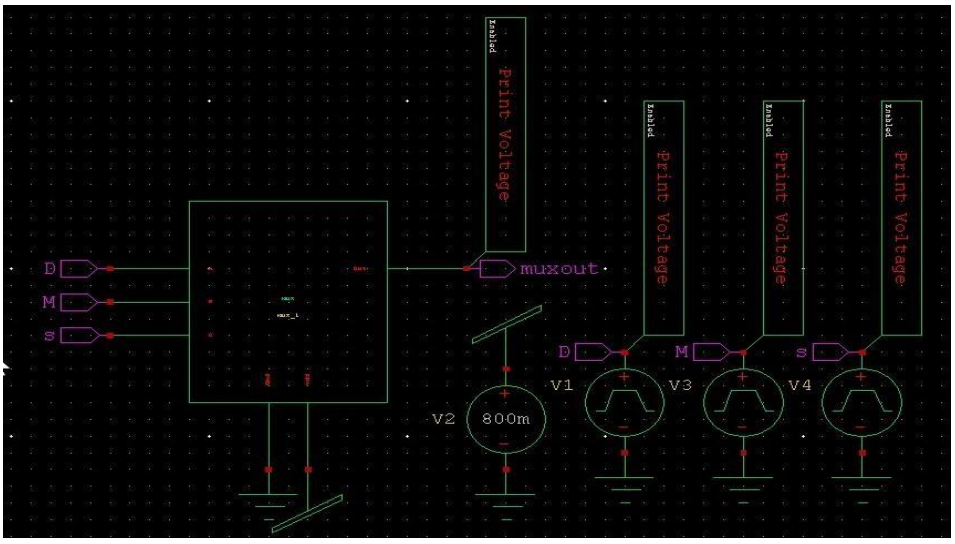

Fig 5.3: Schematic for 2 x 1 Mux

The 2x1 is a fundamental circuit which is also known 2-to-1 multiplexer that are used to choose one signal from two inputs and transmits it to the output. The 2x1 mux has two input lines, one output line, and a single selection line. It has various applications in digital systems such as in microprocessor it is used to select between two different data sources or between two different instructions. A 2x1 multiplexer (mux) is a digital circuit that selects one of two input signals and directs it to the output, based on a single select line.

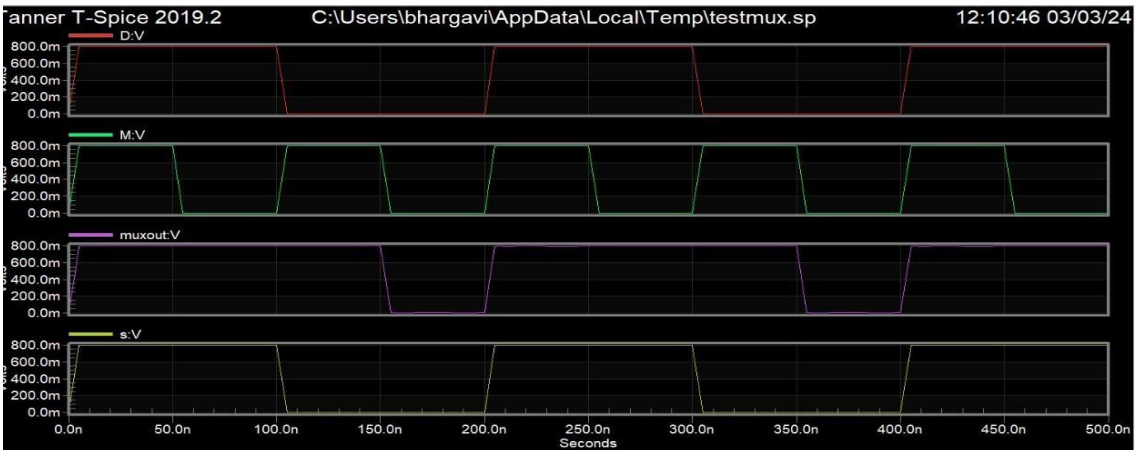

Fig 5.4: Simulation results of 2 x 1 Mux

A 2x1 multiplexer, often abbreviated as a 2:1 MUX, is a fundamental combinational logic circuit in digital electronics. It acts essentially as a data selector or a digital switch. The "2x1" signifies that it has two data input lines and a single output line. To control which of the two input lines is connected to the output, the 2x1 MUX utilizes one additional input called the "select line." This single select line is sufficient because 2^1 = 2, meaning it can differentiate between two distinct input states (0 or 1).

The operation of a 2x1 MUX is straightforward and governed by the state of its select line. Let's denote the two data inputs as I_0 and I_1, the select line as S, and the output as Y. When the select line S is at a logic LOW (typically represented by 0), the data from input I_0 is routed directly to the output Y. Conversely, when the select line S is at a logic HIGH (typically represented by 1), the data from input I_1 is passed through to the output Y. This behavior can be summarized by the Boolean expression Y = S' \cdot I_0 + S \cdot I_1, where S' represents the logical NOT of S.

Due to its simple yet effective data selection capability, the 2x1 MUX is a versatile building block in various digital systems. It can be used for selecting between different data sources, implementing basic logic gates (like AND, OR, NOT), or even as a component in constructing larger multiplexers. Its widespread use in applications ranging from microprocessors to communication systems highlights its importance in efficiently managing and routing data within digital circuits.

6-CONCLUSION

Timing-error resilient circuit with EDAC structure is bur geoning for their timing-guardband mitigation and high energy efficiency. However, several challenges emerge in testing newly introduced logic efficiently, hinder the DFT implementation, and increase the test overhead. In this article, we propose a novel DFT-compatible EDAC structure which supports normal EDAC function, scan shift operation, and purposive timing error generation as well as observation for the test. Benefiting from the testability of hardware design, a set of the shift-based test method is also proposed to test the EDAC structure with low pattern complexity and test time overhead.

The implementation of in-situ timing error detection and correction (EDAC) structures represents a significant advancement in modern digital circuit design, addressing the growing challenges posed by process variations, environmental fluctuations, and aging effects in advanced semiconductor technologies. By enabling real-time error detection and correction, EDAC enhances system reliability, reduces power consumption, and allows circuits to operate closer to their optimal performance limits.

From a technological perspective, EDAC structures provide a more efficient alternative to traditional static guard-banding techniques by dynamically adapting to variations in circuit conditions. This leads to improved energy efficiency, better resource utilization, and enhanced system robustness, making EDAC a crucial component in high-performance and low-power applications. However, the implementation of EDAC comes with challenges, such as design complexity, additional circuit overhead, and power considerations, which require further optimization.

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