International Journal of Multidisciplinary Engineering in Current Research - IJMEC
Volume 10, Issue 6, June-2025, http://ijmec.com/, ISSN: 2456-4265

Synchronous Up Counter with CMOS Clock-Gated Control, Compact Toggle Flip-Flop, and Fast Local Clock Generation

Ms. S Surekha, Mynampati Aarthi, Gangapurapu Abhinaya, Karra Gouthami
[1]Assistant Professor,ECE Department Bhoj Reddy Engineering College for Women
[2,3,4]Ug Scholors, Department Of ECE, Bhoj Reddy Engineering College For Women, India.

ABSTRACT

The clock signal in a counter consumes one-third of the total power. The number of switching actions is minimized in this study to decrease power consumption. The counter's power consumption was reduced even further by decreasing the power consumption of the flip-flops. Combining TSPCL (True Single Phase Clock Logic (TSPCL) with SVL (Self-Controllable Voltage Level) may accomplish this. The Flip-Flop operation is performed by TSPCL at a fast speed and low power. The SVL approach reduces the complexity of the system by suppressing the power generated by leakage current and using fewer transistors. The new design uses low percent less energy than the current one. The suggested technique identifies potential applications for low-power contemporary electronics. To validate proposed design using Cadence virtuoso 45nm Technology. Tool have been used.

1-INTRODUCTION

Synchronous counters have been widely used in digital circuits including programmable frequency dividers for adjusting clock frequency, cost- efficient on-chip . Recently, they are also popularly used in mixed-signal circuits such as clock and data recovery (CDR) circuits, low-power analog-to-digital converters (ADCs), and various compact ultra-low-power synchronous timers for mobile and environmental applications . In these designs, synchronous counters with high speed and lower power are commonly required. A synchronous counter can be implemented with half adders and D flip-flops (DFFs) . It has a simple structure and requires a small number of transistors. But, the counter has disadvantages that may not let it be useful for high-speed and low-power applications. For example, the operating speed of a synchronous counter may not be so high due to a long propagation delay along ripple carry chain paths. The ripple effect becomes severer as the number of counter bits increases. The switching power consumption can also be unnecessarily high due to a large number of redundant transitions at higher-weight counter bits. To address the issue of speed degradation, using a high-speed carry chain circuit can be a solution for counters having their bit width in a medium range (16 to 64) . But due to extra circuits required, a large overhead in terms of power and area is an issue. In applications requiring counters having a wide bit width, a linear feedback shift register (LFSR) can be used as a state generator to enhance the counting speed. However, it still occupies large area and dissipates a large amount of redundant power during counting operation. To address the issue of the redundant power consumption, a low-power technique such as the clock gating can be used. In the clock-gating scheme, the clock signal is enabled only when a valid computation is required. When the computation result is not useful, the clock signal is gated to be disabled, resulting on no transitions. The technique can reduce the overall power consumption by eliminating redundant transitions in circuit blocks and through a clock-gating logic. In this approach,

internal clock signals are allowed to toggle only when data transitions are required. However, such schemes have a limitation of device count overhead since they require extra transistors for implementing the clock gating logic. Other schemes which can minimize the power consumption by reducing the redundant transitions of flip-flops themselves were also presented . The Four-bit up counting sequence the reduction techniques can be applied but they also have limitations due to the power- area trade-offs. To overcome these limitations, a pulse-based clock-gated synchronous counter has been proposed. The counter can minimize power consumption by efficiently eliminating all redundant transitions in the circuit by embedding a clock gating scheme in the carry propagation circuit. Using this approach, no extra circuits are required to eliminate redundant transitions, and the total device count becomes even smaller than one without clock gating, resulting in a substantial area and power reduction with marginal speed improvement. But, the scheme still has limitations that the carry propagation delay increases substantially as the number of counter bit increases, and that the down-counting operation cannot be supported. Moreover, flip-flops storing counter bits are not optimized, wasting additional power and area. To address the issues of conventional synchronous counters in terms of speed and power described above, a speed enhanced clock- gated synchronous up/down counter is proposed. The contributions of the paper are as follows. For speeding up the counting operation, the high-speed carry selection technique is adopted. The use of a single set of Manchester carry chain for this purpose can minimize overheads in terms of power and area. Noticing that in our counter having a clock gating along the carry propagation path local clock transitions always imply flip-flop state transitions, a compact toggle flip-flop is designed, resulting in further power and area reduction. A methodology used in digital circuit design is called TSPCL with SVL. This technique combines the TSPCL approach with the SVL technique to enhance the performance and efficiency of the circuit. The Flip-Flop operation is executed by TSPCL at a high speed while consuming low power. The SVL technique effectively mitigates power caused by leakage current and achieves a reduction in the number of transistors, resulting in decreased system complexity. When compared to the present design, the proposed solution consumes 27% less electricity. The suggested technique includes potential opportunities for the development of energy-efficient modern electronic devices. The SVL module verifies the results by relying on the outcomes of TSPCL. The proposed architecture incorporates a structured VLSI methodology, which enables the derivation of area through an analytical method that relates the transistor count and the total delay in terms of operand bit width. Specter simulations were conducted using 0.18 micron CMOS technology operating at a frequency of 1 GHz. With the implementation of the proposed design, power consumption was observed to decrease by 290.3% in nano watts, while power delay was reduced by 20.23% when compared to the existing model.

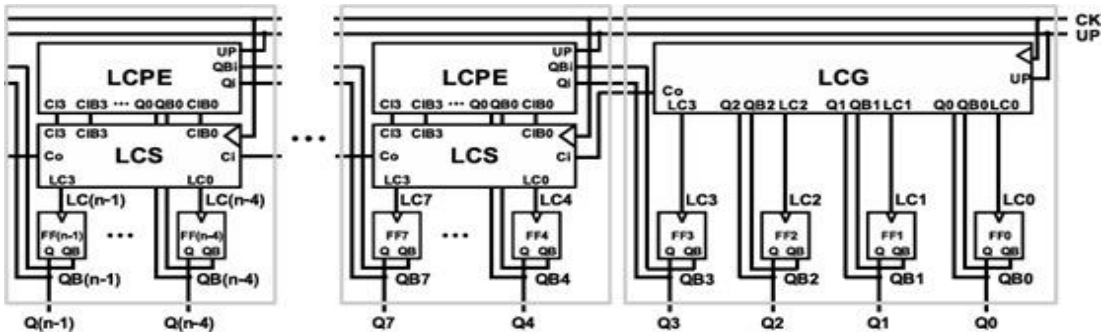
2-SOFTWARE REQUIREMENT

The proposed Synchronous Up Counter with CMOS Clock-Gated Control Compact Toggle Flip-Flop and a Fast Local Clock Generation was designed and implemented using industry-standard electronic design automation (EDA) tools.

The circuit's full schematic design, simulation, and functional verification were all done using the Cadence tool i.e. CADENCE 45NM GPDK. To ensure accuracy and dependability, Cadence was used

to conduct a thorough transistor-level analysis of the circuit's timing Behavior, power analysis, and overall performance.Tanner EDA was used for layout design and post-layout verification. Tanner performed Layout Versus Schematic (LVS) verification, Design Rule Check (DRC), and circuit layout design. This guaranteed that the physical design adhered to fabrication design constraints and matched the schematic.

3-EXISTING METHOD



The overall block diagram of the counter is divided into circuit segments, each having four counter bits. The least significant bit (LSB) segment has a local clock generator (LCG), and other segments have local clock pre-evaluators (LCPEs) and local clock selectors (LCSs). In each segment, there are flip-flops for storing the counter bits. LCG is used to generate pulsed local clocks (LC0-LC3) for four lower-weight counter bits. LCPEs pre-evaluate higher-weight carries before the arrival of the carry inputs propagated from lower-weight bit positions. LCSs generate valid local clocks (LC4-LC(n-1) where n indicates the number of counter bits) for higher weight counter bits from LCPE outputs using incoming carry inputs. These pulsed local clocks are used for counter-bit updates as the counting operation advances.

4-PROPOSED METHOD

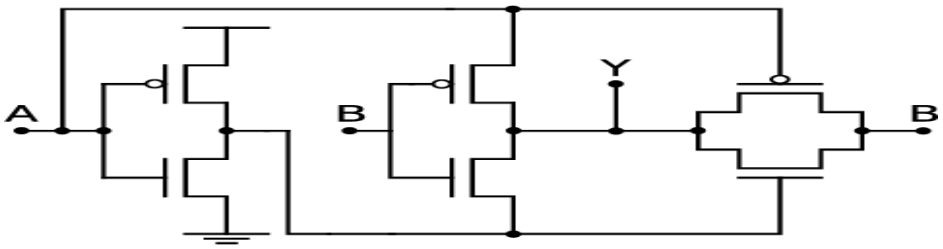


Fig: Transmission Gate Design XOR gate

The truth table for the 'XOR' gate is displayed in the following table: The diagram depicted in Figure Above illustrates the utilization of pass transistors to implement the 'XOR' function. In this gate, when the B input is at a low logic level, the left NMOS transistor is activated, allowing the logic value of A to be transferred to the output F. When the B input is set to a high logic level, the NMOS transistor is turned on, allowing the inverted logic value of A to be transferred to the output F. This configuration ensures that the truth table of the XOR gate is satisfied. The circuit depicted in Figure 2 represents a two-input XOR circuit implemented using CMOS technology. The NOR gate is formed

by MOSFETs Q1, Q2, Q3, and Q4. Q5 and Q6 execute the logical AND operation between inputs A and B, while Q7 performs the logical OR operation between the outputs of the NOR and AND gates.

The digital logic gate under consideration is designed to produce a true output only when the genuine input count is an odd amount (represented by 1 or HIGH). The logical XOR gate operates by carrying out the exclusive or operation. The XOR gate is a logical operator in mathematics that returns a true value if and only if any one of its inputs is also true. When both inputs are either false (0/LOW) or true, a false output is generated. Inequality is represented by the XOR operation. The result is true if and only if the inputs are unique, and false otherwise. One method to recall the concept of XOR is by remembering the phrase "must possess either one or the other, but not both." With the XOR gate, one input may determine if the other is inverted, making it a "programmable inverter" or passed through without any alteration. Therefore, it operates as an inverter, specifically a NOT gate, that can be toggled on or off using a switch.

The XOR operation is equivalent to a modulo-2 addition. In computers, XOR gates are frequently used to make binary addition easier to implement. Two logic gates, an exclusive- or (XOR) gate and an addition (AND) gate, make up a half adder. The gate is also used in comparators and subtractors .consumes lesser power with maximum reliability The user's text is too short to rewrite in a technical writing style. The dissipation can be further divided into static and dynamic components. The latter phenomenon exclusively takes place during transients, specifically when the gate is in the process of switching Capacitor charging and the resulting temporary current pathways between the supply rails are directly responsible for the dynamic power consumption that results. As the number of switching events grows, so does the dynamic power consumption; the two are proportional to one another. The static component, in contrast, remains present even in the absence of switching and is attributed to static conductive paths between the supply rails or leakage currents. The presence of the circuit is constant, even during stand-by mode. The goal of minimizing this consumption source is considered to be worthwhile. Since the propagation delay is proportional to the rate at which a given amount of energy can be stored on the gate capacitors, power consumption is directly related to the propagation delay. The speed of the gate is directly proportional to the rate of energy transfer or power consumption. In the context of a specific technology and gate topology, The product of power usage and delay in propagation is relatively constant, as has been observed. At higher frequencies, the suggested SRAM cell shows almost constant dynamic power dissipation. The use of voltage sources improves the SRAM cell's stability by increasing its switching capabilities. In order to reduce current leakage throughout transition modes, the self-controllable voltage level approach is used. Because of this decrease in leakage current, the proposed SRAM cell has lower static power dissipation. In the realm of VLSI circuits, low power testing has become an important consideration. This paper takes a fresh look at the design of a scan cell fora True Single Phase Clock (TSPC). During scan shifts, the design priorities minimizing clock signal loading and power consumption in the combinational circuit. The initial module is the Comparison True Single Phase Clock (TSPCL), while the subsequent module is the Self-Controllable Voltage (SVL). Based on the idea of genuine single phase operation, the true single phase scan flip-flop places the least amount of load on the

clock signal possible. During a serial scan, the scan flip-flop effectively disables any unneeded transitions.

Fig: 4 -bit synchronous counter

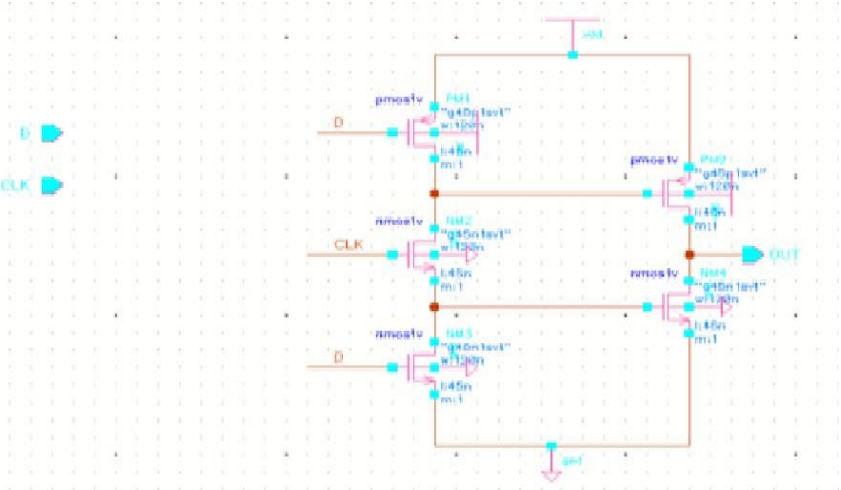


Fig: D Flip Flop

SVL LOGIC

The Self Controlled voltage level (SCVL) technique can be employed as a control circuit in two ways. To begin, it can be employed at the upper end of the unit to reduce the supply voltage, a technique known as the U-SVL technique. Secondly, it can be utilized at the lower end of the unit to elevate the potential of the ground node, referred to as the L-SVL technique. The Upper SVL configuration comprises a single PMOS1V (PM13) and two NMOS 1V transistors (NM12, NM14) connected in series. The "on-pmos1v" is responsible for establishing a connection When the MUX circuit is in active mode, it communicates with the power supply (VDD). When the MUX circuit is in standby mode, the "on-nmos1v" connects the power supply (VDD) to it. Two N-channel Metal-Oxide-Semiconductor (NMOS) transistors are connected in series at the highest Source Voltage Level (SVL), and a P-

channel NMOS transistor is connected in parallel at the same SVL. Two NMOS transistors, one each linked to the power source and the inverted input clock, share a PMOS transistor's gate. When the clock signal (clk) is set to 1, the complementary clock signal (clkb) is inverted to 0, causing the PMOS transistor to turn on. The PMOS transistor becomes conductive, allowing the supply voltage 1 to flow through it. When the clock signal (clk) is at a logic low state (0), the complementary clock signal (clkb) transitions to a logic high state (1). This transition causes the two NMOS transistors to enter

a conducting state, establishing a connection to the ground. The reduction of leakage power in the off condition of the circuit can be achieved by connecting the NMOS devices in series. This document presents the design specifications for the Upper SVL.

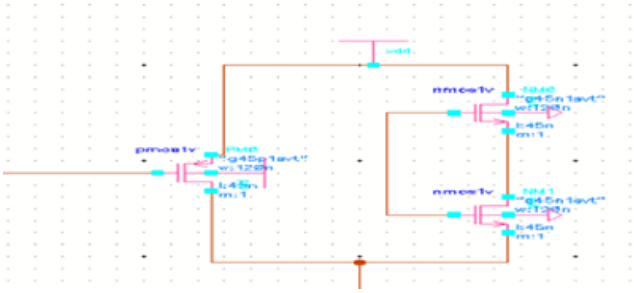


Fig: Upper SVL Design.

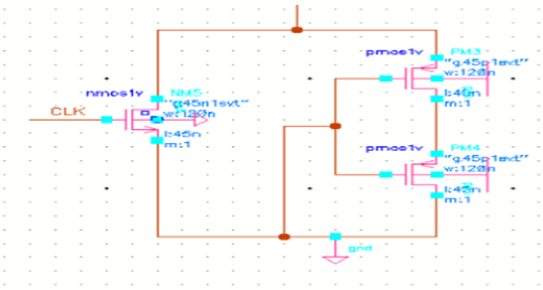


Fig: lower SVL Design.

5-RESULTS AND DISCUSSION

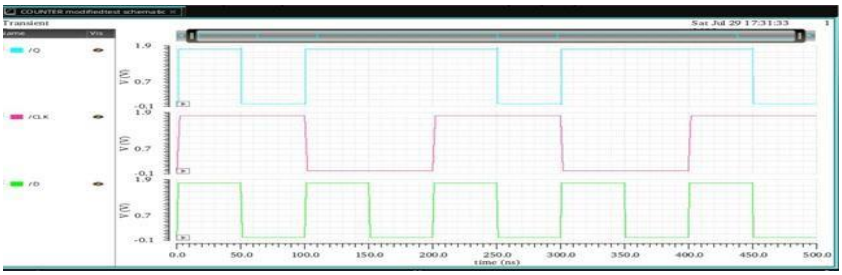


Fig: Modified D ff with USVL LSVL simulation

Recital CMOS D Flip-Flop circuits are used often in both digital and analog applications. The evaluation of leakage power is of paramount importance in the realm of CMOS technology. When the circuit is not actively using power, the supply voltage can be lowered to save energy and prolong the battery's life. In order to reduce signal interference, the CMOS D Flip- Flop circuit uses the Modified SVL approach and minimize power dissipation caused by leakage currents. The modified design utilizes a minimal number of transistors, resulting in a reduction in the consumption of dynamic power.

4-Bit counter circuit and simulation:

Upon completion of the aforementioned gates and

circuit, it is now possible to integrate them into a comprehensive 4-Bit comparator. The test bench schematic of the 4-Bit comparator is shown in Figure.

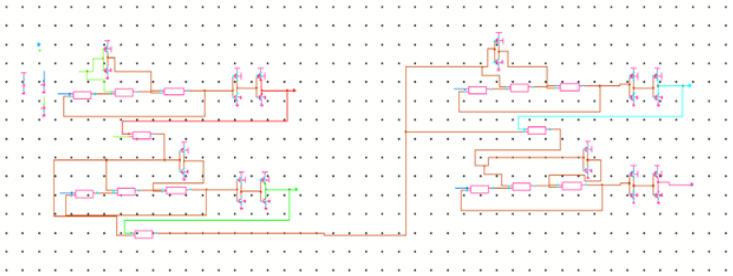


Fig: proposed schematic of 4 Bit Counter

With the use of clock gating, a new power-efficient simultaneous counter has been developed. Only when the Flip-Flops are in their active state can the clock be toggled. This method solves the problem of circuit complexity efficiently. The following is a schematic depiction of a conventional 4-bit binary increment counter. The design has shown that it can work with many different sizes of data. A clock signal is sent from the clock network to the Flip Flop. The network's repeaters are set up in a sequence, which helps reduce clock skew. By using combinational logic to regulate the clock based on Flip-Flop operations, the circuit provides the benefit of low power consumption in the clock network. Flip-Flop power savings may be maximized by disabling its clock while it is not in use. The schematic for a 4-Bit Existing Binary Up Counter is detailed here. The suggested layout makes use of a Flip-Flop that is activated by a rising edge. When compared to a standard Flip-Flop, the TSPCL coupled with the SVL approach results in a significant reduction in power consumption. A combined SVL T Flip-Flop design is presented in this publication. P1 is in the active state, N2 is also in the active state, while P2 and P3 are in the inactive state. Both N1 and N2 are currently not in use. To facilitate the standard operation of the D Flip-Flop, it is essential to establish connections with the power supply and ground (GND). When the component labeled "a" is in an inactive state, the components labeled P1, N1, and N3 are in an active state, while the components labeled P2 and N2 are in an inactive state. As a result, the output also becomes inactive. When the value of variable "a" is set to 1, it causes P1 and N3to to transition to an inactive state, while N1, N2, and P2 transition to an active state, resulting in the output becoming one. P1 and N3 are in the OFF state, meaning that they are open circuits. N1 and N2 are in an active state, functioning as a pull-up network. As a result, the supply voltage is Vdd-Vth. Connecting NMOS transistors in series results in a reduction of static power.

Simulation Results of Flip-Flop and Counter

The suggested T Flip-Flop design was simulated with TSPCL and SVL, and the results are shown below.

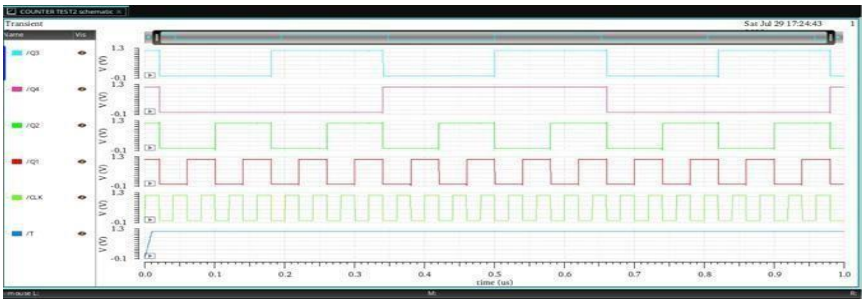


Fig: proposed of 4 Bit counter simulation

The input variable is represented by "b," and the result is "Q." The clock input is also labeled "CLK." If the input is 0 at the time the clock is rising, the output will also be 0. Until the next time the clock rises, this output will not change. The given bit is set to a value of 1 upon the occurrence of the second rising edge. The outcome is a 0/1 state transition at the output. As a result, there is no change in output at the falling edge. When the input is 1, the output changes state from 1 to 0 on the third rising edge. This condition lasts until the next trough in the wave's trajectory. If the input is a 1 at the next rising edge, the output will be switched between 1 and 0 at the same time. After that, the output will stay constant until the falling edge of the clock signal.

Table comparison of proposed and existing method

S.NO	Method	Power (nW)	Delay (nsec)	No.ofTransistors (area)
1	Existing Method	3.27	20.73	186
2	Proposed	2.18	13.23	140

Power analysis

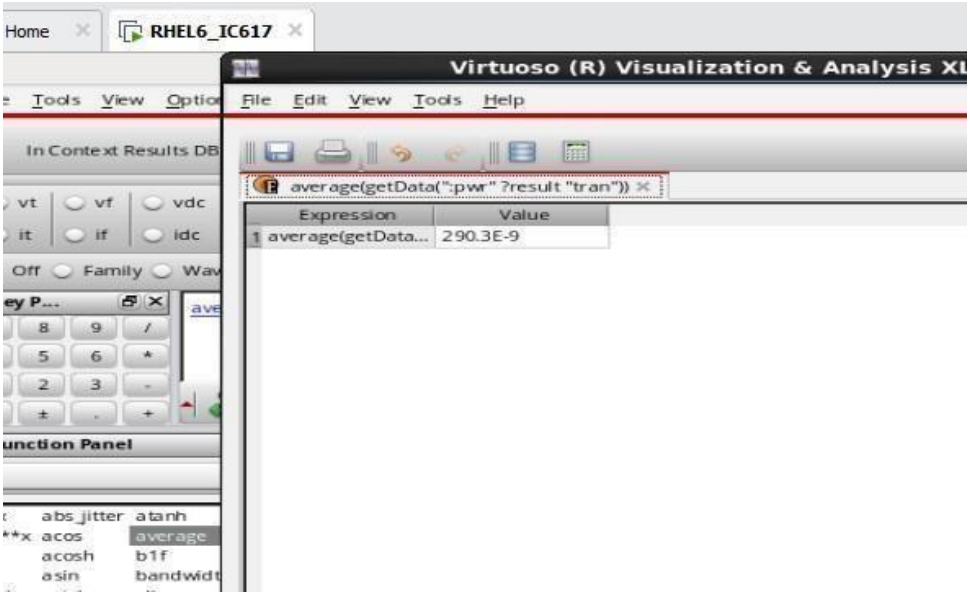


Fig: Average power 290.3 nano watts

The suggested Flip-Flop design has been shown to reduce power dissipation in experiments. When compared to the power dissipation of the standard Flip-Flop design, this one uses 30% less energy at 2.5V, 19% less at 3V, 44% less at 3.5V, 45% less at 4V, 23% less at 4.5V, and 18% less at 5V. The counter design's power dissipation result. Taking into account supply voltages between 2.5V and 5.0V, this research evaluates the power dissipation outcomes of both the present counter and the new counter.

Delay Analysis

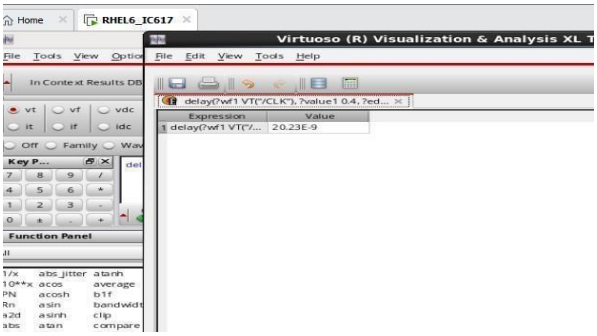


Fig: Delay 20.23 nano seconds

Counter layout

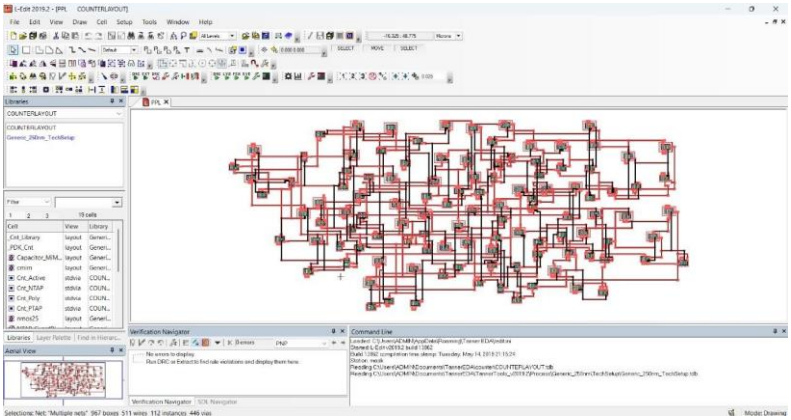


Fig: Counter layout

Fig: Counter area

6-CONCLUSION

The utilization of power in the counter is reduced through the implementation of the suggested T Flip-Flop with clock gating technique. The T Flip-Flop is created by integrating the TSPCL and SVL techniques. The proposed T Flip-Flop design

demonstrates a power consumption of only 0.34 microwatts, representing a 30% reduction compared to the power usage of the current T Flip-Flop design. When compared to the current counter design, the suggested counter design shows a 27% reduction in power usage. Using the Tanner Tool and simulating with 250nm CMOS technology, a T Flip-Flop and counter with anticipated performance have been created and simulated. The suggested counter is intended to use as little energy as possible while also taking up as little space on the chip as possible. TSPCL, Upper and Lower SVL are all used in the building of counters, and their use together illustrates that it is possible to use them together in the design of energy- efficient Flip-Flops. The suggested architecture is tailored to the requirements of a 4-bit incrementing counter. However, it may be modified to allow for the development of low-power, wide-bit counters. The goal of this work is to compare the efficiency of counter and Flip-Flop circuits. Area and delay analysis of Flip- Flop and counter designs at different Supply Voltages are also possible. The proposed counter layout uses 27% less energy than the current counter. Future work involves the continued reduction of power consumption in the counter, with the aim of achieving even lower power levels than those proposed in the current counter design.

REFERENCES

[1].G. Theodoridis and A. Kakarountas, "High speed binary counter based on 1d cellular automata," 5th International conference on modern circuits and systems technologies (MOCAST), Thessaloniki, pp. 1–4, 2016.

[2]K. Gavaskar and U S. Ragupathy, "Low power self-controllable voltage level and low swing logic based 11T SRAM cell for high speed CMOS circuits," Springer, Vol. 100, No. 1, pp. 61-77, 2019.

[3]T. Doi, and V. Niranjan, "Low power and high performance ring counter using pulsed latch technique," International conference on micro-electronics and telecommunication engineering (ICMETE), Ghaziabad, pp.584–586, 2016.

[4]M. Gautam, U. Nirmal and R. Jain, "Low power sequential circuits using improved clocked adiabatic logic in 180nm CMOS processes,
International conference on research advances in integrated navigation systems (RAINS), Bangalore, pp.1–4, 2016.

[5]K. Gavaskar, U S. Ragupathy and V. Malini, " Design of Novel SRAM cell using Hybrid VLSI Techniques for Low Leakage and High Speed in Embedded Memories," Springer, Vol. 108, No.4, pp.2311-2339, 2019.

[6]JS. Kim, JO. Yoonand and B D. Choi, " Low-power counter for column-parallel CMOS image sensors," IEEE Asia Pacific conference on circuits and systems (APCCAS), Jeju, pp.554–556, 2016.

[7]K. Gavaskar and U S. Ragupathy, " An efficient design and analysis of low power SRAM memory cell for ULTRA applications," Asian journal of research in social sciences and humanities, Vol. 7, pp. 962- 975, 2017.

[8] Madhu Shakya and Shweta Agrawal, "Design of Low Power C-MOS D flip- flop using modified SVL technique," International Journal of Research and Analytical Reviews, Vo. 5, No. 4, pp. 2349-5138, 2018.

[9]K. Gavaskar and U S. Ragupathy, "An efficient design and comparative analysis of low power memory cell structures," IEEE International conference on Green Computing, Communication and Electrical Engineering (ICGCCEE'14), pp. 489-493, 2016.